

MS-7509

VER 20
uATX(244mm X 200mm)

CPU:

AMD AM2+ / AM3 Socket940

System Chipset:

North Bridge --- MCP78V

South Bridge --- NA

OnBoard Chipset:

Clock Gen:NA

AC'97 Codec:ALC888

LAN Chip: REL8211BL/8201CL

SIO:Fintek 882(with smart fan control-3/4 pin co-lay)

Flash ROM:8MB SPI (SIO)

Main Memory:

DDRII* 2 (Dual Channel)

Expansion Slots:

PCI Express (X16) Slot * 1

PCI Express (X1) Slot * 1

PCI Slot * 2

PWM:

Controller:ISL6566

ACPI:

UPI solution

Other:

FDD *1

SATA(SATA2-300MB/s) * 6(included 1 ESATA)

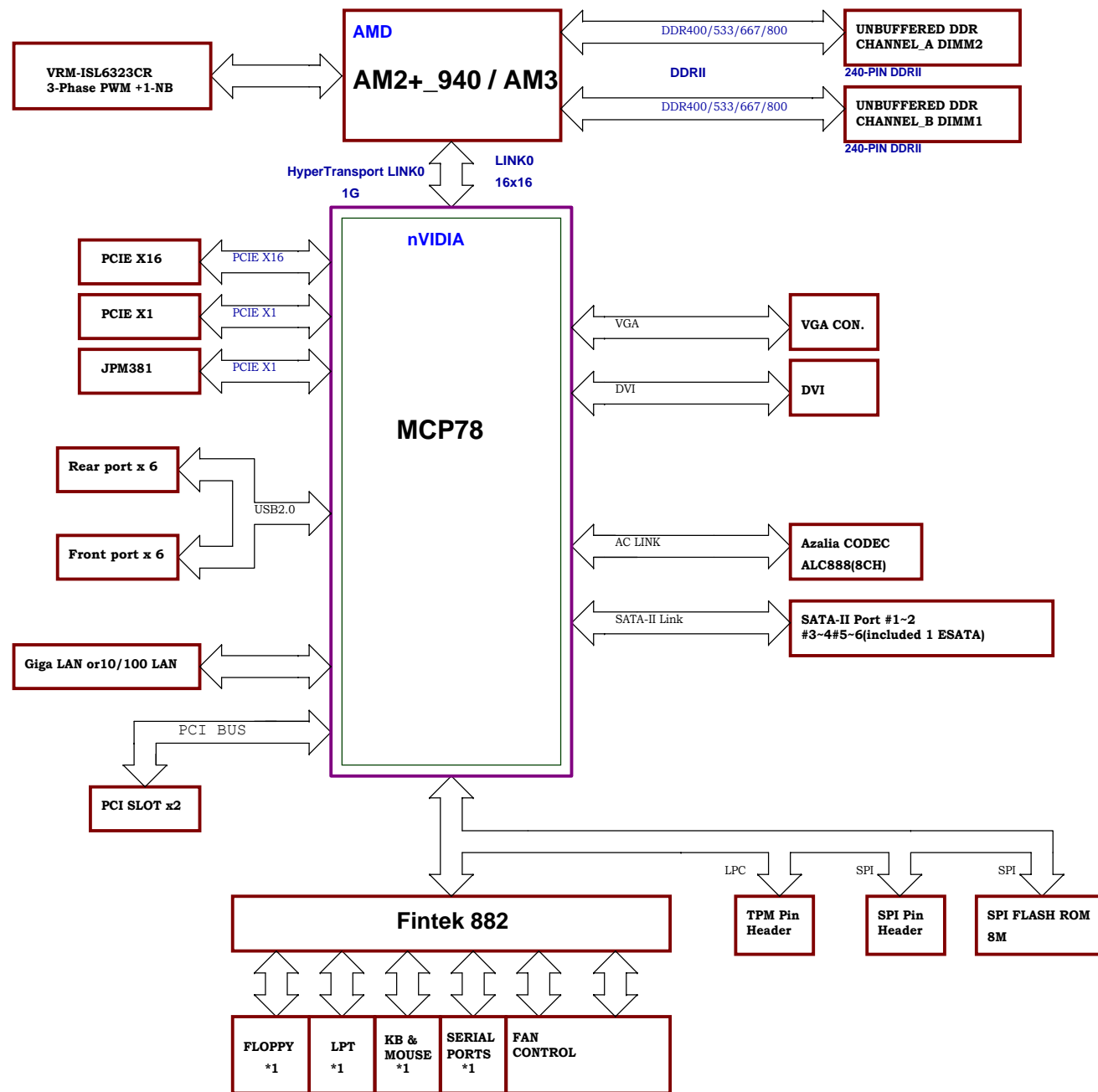
USB2.0 *12 (Rear*6 Front*6)

COM PORT *1

LPT PORT *1

DVI*1

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| CPU: AM2+ | 6,7,8,9 |
| DDR2 DIMM(Dual Channel) | 10,11,12 |
| MCP78 | 13 ~ 19 |
| LAN_ RTL8211BL/8201CL | 20 |
| PCIE x 16 , x1 Slots. | 21 |
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DDR DIMM Config.

| DEVICE | ADDRESS | CLOCK |
|----------------|-----------|-------------------|
| DIMM 2 CH-A | 10100000B | MEM_MAO_CLK_H0/L0 |
| | | MEM_MAO_CLK_H1/L1 |
| | | MEM_MAO_CLK_H2/L2 |
| DIMM 1 CH-B | 10100001B | MEM_MBO_CLK_H0/L0 |
| | | MEM_MBO_CLK_H1/L1 |
| | | MEM_MBO_CLK_H2/L2 |

| USB | Port | DATA +/- | OC# |
|-------|-------------|--------------------------------------|-----|
| Rear | ESATA_USB1A | USB0- USB0+ USB1- USB1+ | |
| | I1394_USB1 | USB2- USB2+ USB3- USB3+ | |
| | LAN_USB1A | USB10- USB10+ USB11- USB11+ | |
| Front | JUSB4 | USB4- USB4+ USB5- USB5+ | |
| | JUSB2 | USB6- USB6+ USB7- USB7+ | |
| | JUSB5 | USB8- USB8+ USB9- USB9+ | |

PCI Config.

| DEVICE | MCP1 INT Pin | REQ#/GNT# | IDSEL | CLOCK |
|------------|--|------------------------|-------|--------------------------|
| PCI Slot 2 | PCI_INT#X PCI_INT#Y PCI_INT#Z PCI_INT#W | PCI_REQ2# PCI_GNT2# | AD25 | PCICLK2 (PCI_CLK2) |
| PCI Slot 1 | PCI_INT#W PCI_INT#X PCI_INT#Y PCI_INT#Z | PCI_REQ3# PCI_GNT3# | AD24 | PCICLK1 (PCI_CLK1) |
| IEEE1394 | | | | PCIE2_CLK /PCIE2_CLK# |
| TPM | | | | LPCCLK (LPC_CLK1) |
| Chipset | | | | PCI_CLKIN (PCICLK4) |
| LPC | | | | LPC_PCLK |
| SIO | | | | SIOPCLK (LPC_CLK0) |

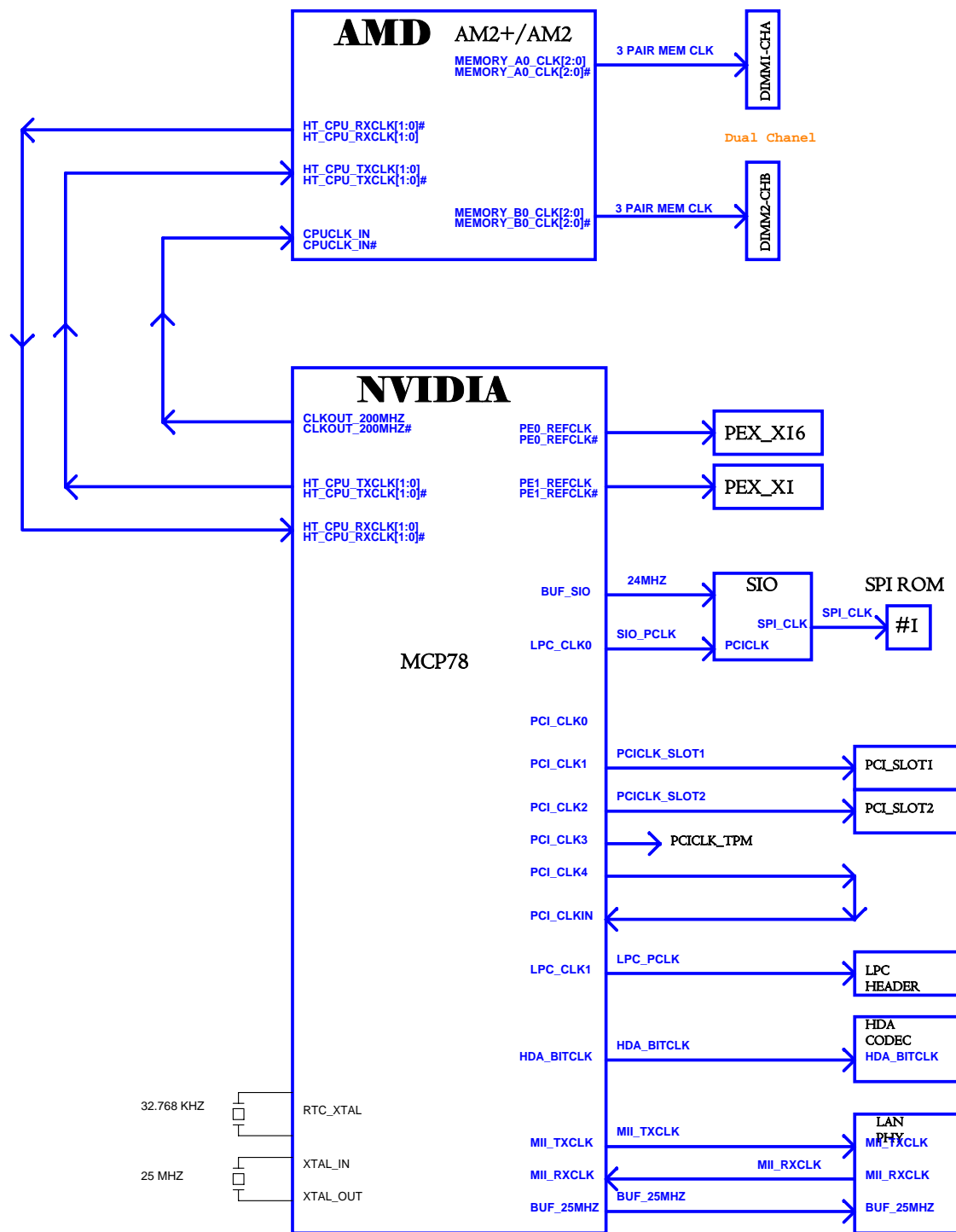
| CPU VID TABLE | |
|---------------|---------|
| VID | VOLTAGE |
| 00000 | 1.5500V |
| 00001 | 1.5250V |
| 00010 | 1.5000V |
| 00011 | 1.4750V |
| 00100 | 1.4500V |
| 00101 | 1.4250V |
| 00110 | 1.4000V |
| 00111 | 1.3750V |
| 01000 | 1.3500V |
| 01001 | 1.3250V |
| 01010 | 1.3000V |
| 01011 | 1.2750V |
| 01100 | 1.2500V |
| 01101 | 1.2250V |
| 01110 | 1.2000V |
| 01111 | 1.1750V |
| 10000 | 1.1500V |
| 10001 | 1.1250V |
| 10010 | 1.1000V |
| 10011 | 1.0750V |
| 10100 | 1.0500V |
| 10101 | 1.0250V |
| 10110 | 1.0000V |
| 10111 | 0.9750V |
| 11000 | 0.9500V |
| 11001 | 0.9250V |
| 11010 | 0.9000V |
| 11011 | 0.8750V |
| 11100 | 0.8500V |
| 11101 | 0.8250V |
| 11110 | 0.8000V |
| 11111 | 0.7750V |

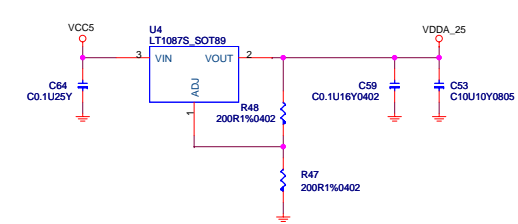
PCI RESET DEVICE

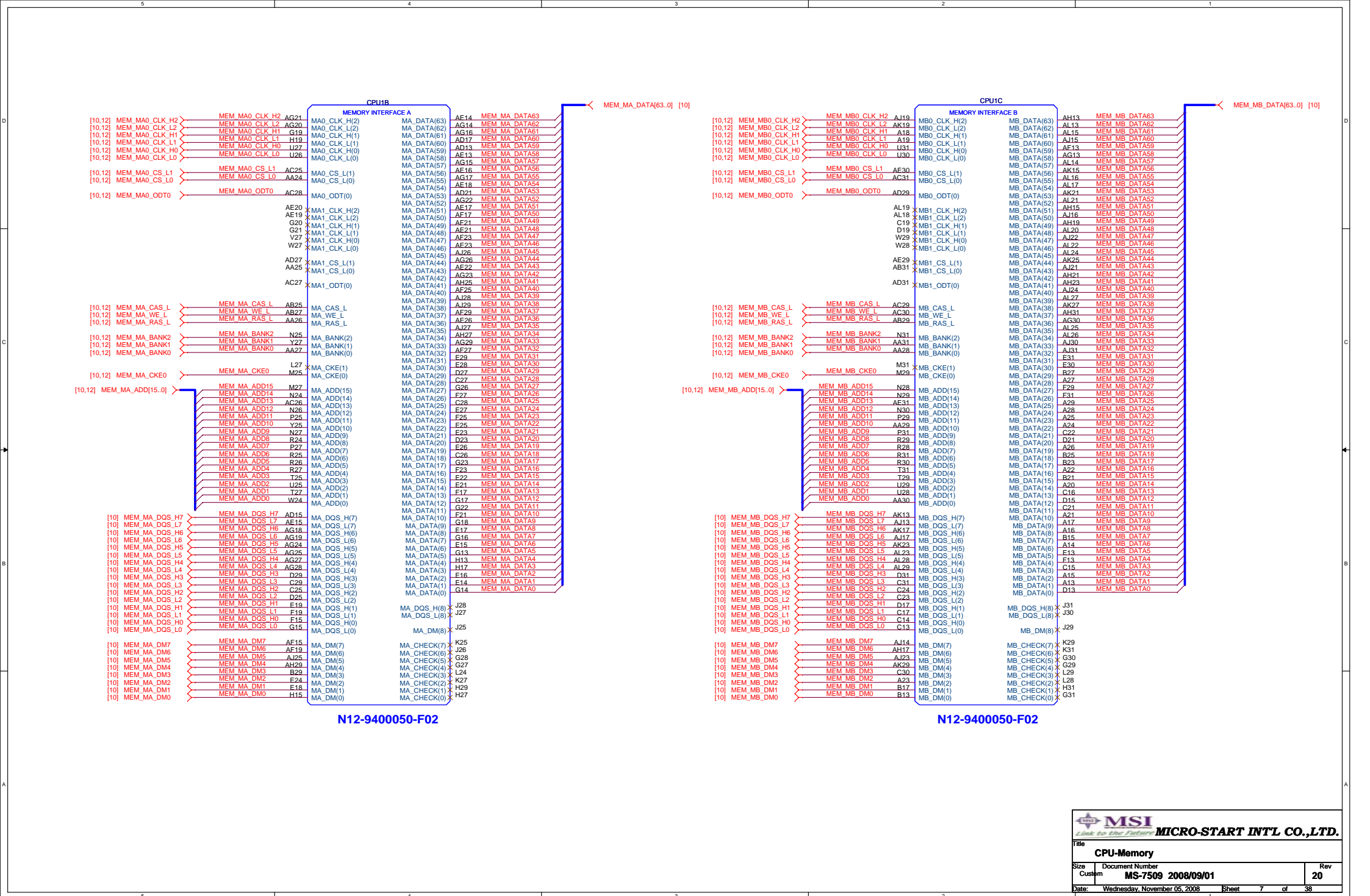
| MCP78 | |
|-------------|---------------|
| Signals | Target |
| PCI_RESET0* | PCIRST_SLOT1# |
| PCI_RESET1* | PCIRST_SLOT2# |
| PCI_RESET2* | HD_RST# |
| PCI_RESET3* | JTPM_RST# |
| LPC RESET* | SIO_RST# |

| MCP78 GPIO TABLE | |
|---|--|
| PIN NAME | FUNCTION |
| THERMTRIP*/GPIO58 PROCHOT*/GPIO20 | CPU_THERMTRIP* PROCHOT* |
| MII_RXER/GPIO36 MII_COL/GPIO13/MI2C_DATA MII_CRS/GPIO14/MI2C_CLK RGMII/MII_INTR*/GPIO35 RGMII/MII_PWRDWN*/GPIO37 MII_RESET*/GPIO12 | MII_RXER MII_COL MII_CRS Pull High 10K to 3VDUAL -- MII_RESET* |
| DDC_CLK/GPIO17 DDC_DATA/GPIO19 | DDC_CLK DDC_DATA |
| PCI_REQ2*/GPIO40.RS232_DSR* PCI_REQ3*/GPIO38.RS232_CTS* PCI_GNT2*/GPIO41.RS232_DTR* PCI_GNT3*/GPIO39.RS232_RTS* PCI_PERR*/GPIO43.RS232_DCD* PCI_PME*/GPIO30 LPC_PWRDWN*/GPIO54/EXT_NMI* LPC_DRQ0*/GPIO50 LPC_DRQ1*/GPIO15/FANRPM1 | PCI_REQ2* Pull High to 3VDUAL PCI_REQ3* Pull High to 3VDUAL PCI_GNT2* PCI_GNT3* PCI_PERR* PCI_PME* OD_TCK LPC_DRQ0* -- |
| CABLE_DET_P/GPIO63 SATE_LED*/GPIO57 | CABLE_DET_P SATE_LED* |
| HDA_SDATA_OUT0/GPIO45 HDA_SDATA_IN0/GPIO22 HDA_SDATA_IN1/GPIO23/MGPIO0 HDA_SYNC/GPIO44 GPIO_1 GPIO_2/NMI*/PS2_CLK0 GPIO_3/SMI*/PS2_DATA0 GPIO_4/SCL_INTR/PS2_CLK1 GPIO_5/INIT*/PS2_DATA2 GPIO_6/FERR*/SYS_FERR* GPIO_7/INFERR*/SYS_PERR* GPIO_8/SPI_DI GPIO_9/SPI_DO GPIO_10/SPI_CS GPIO_11/SPI_CLK USB_OC0*/GPIO25 USB_OC1*/GPIO26 USB_OC2*/GPIO27 USB_OC3*/GPIO28/MGPIO_1 USB_OC4*/GPIO29 A20GATE/GPIO55 EXT_SMI*/GPIO32 RT*/GPIO33 SIO_PME*/GPIO31 KBRDRSTIN*/GPIO56 SUS_CLK/GPIO34 THERM*/GPIO59 FANRPM0/GPIO60 FANCTL0/GPIO61 FANCTL1/GPIO62 THERM_SIC/GPIO48 THERM_SIDO/GPIO49 PE_WAKE*/GPIO21 | HDA_SDATA_OUT HDA_SDATA_IN0 -- HDA_SYNC -- -- -- -- OD_CPU_RST_L DBREQ_L OD_TRST_L -- -- -- -- Pull High 10K to 3VDUAL(USB not USE) Pull High 10K to 3VDUAL(USB not USE) Pull High 10K to 3VDUAL(USB not USE) Pull High 10K to 3VDUAL(USB not USE) Pull High 10K to 3VDUAL(USB not USE) Pull High 10K to 3VDUAL(USB not USE) A20GATE EXT_SMI* G3 TO S5 POEWR CONTROL SIO_PME* SIO_KBRST* -- DO_DBRDY# THERM* -- OD_TDO# Internal 10K pull-up to vcc3 PE_WAKE* |

| SIO GPIO TABLE | | |
|--------------------|--|--|
| GROUP | PIN NAME | FUNCTION |
| UART & SIR | IRTXX/GPIO42 IRRXX/GPIO43 GPIO17 | -- PCI_PERR* DDC_CLK |
| Hardware Monitor | FANIN3/GPIO40 FAN_CTL3/GPIO41 PME#/GPIO25 GPIO10/SPISLK/FININ4 GPIO11/SPI_CS0#/FAN_CTL4 GPIO12/SPI_MISO/FANCTL1_1 GPIO13/SPI_MOSI/BEEP GPIO14/FWH_DIS/WDTRST#/SPI_CS1# | DDC_CLK PCI_GNT2* PME# SPI_SLK SPI_CS0# SPI_RESET* MII_COL MII_CRS |
| ACPI Function Pins | GPIO15/LED_VSB/ALERT# GPIO16/LED_VCC/Turbo2# PCIRST1#/GPIO20 PCIRST2#/GPIO21 PCIRST3#/GPIO22 GPIO23/RSTCON# ATXPG_IN/GPIO24 PWROK/GPIO32 PWSIN#/GPIO26 PWSOUT#/GPIO27 S3#/GPIO30 PSON#/GPIO31 RSMRST#/GPIO33 | SUS_LED PWR_LED PROCHOT* PE_WAKE* HDA_SDATA_IN0 -- ATXPG_IN -- PWSIN# PWSOUT# S3# PSON# -- |
| VID Controller | VIDOUT0/GPIO0 VIDOUT1/GPIO1 VIDOUT2/GPIO2 VIDOUT3/GPIO3 VIDOUT4/GPIO4 VIDOUT5/GPIO5/SIC SLOT0CC#/GPIO6 GPIO7/Turbo1#/WDTRST# | VIDOUT0 VIDOUT1 VIDOUT2 VIDOUT3 VIDOUT4 SIC SLOT0CC# -- |







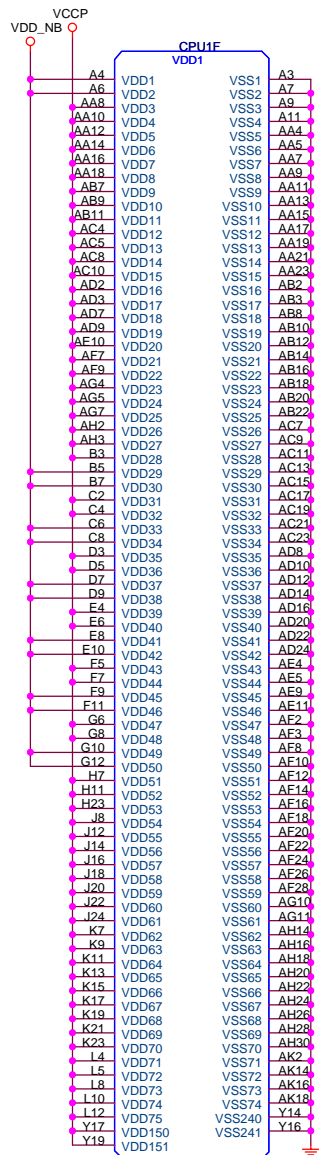
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N12-940050-F02

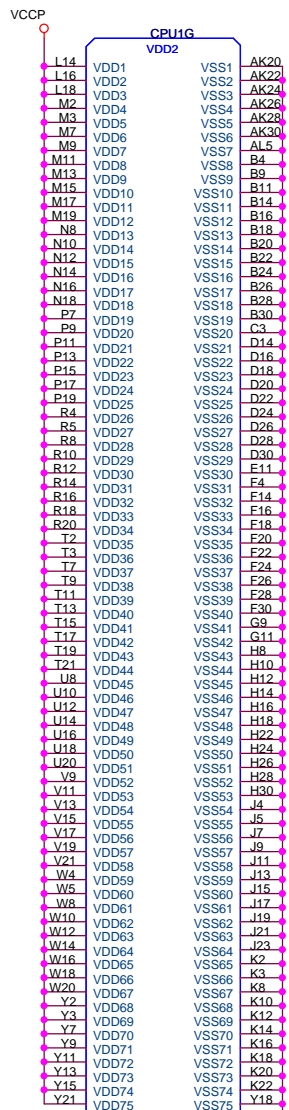
MSI
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Title: **CPU-Memory**

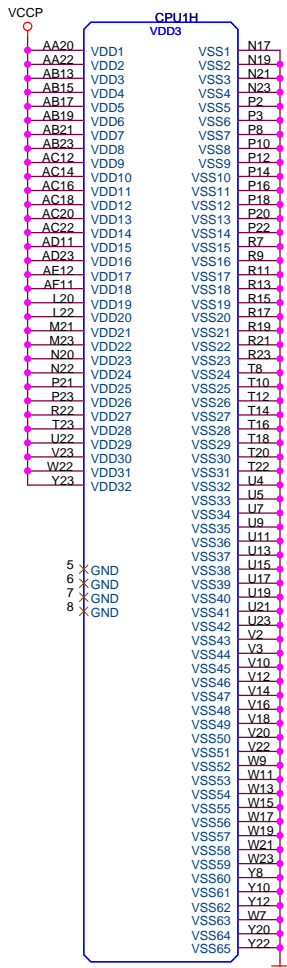
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| Size: Custom | Document Number: MS-7509 2008/09/01 | Rev: 20 |
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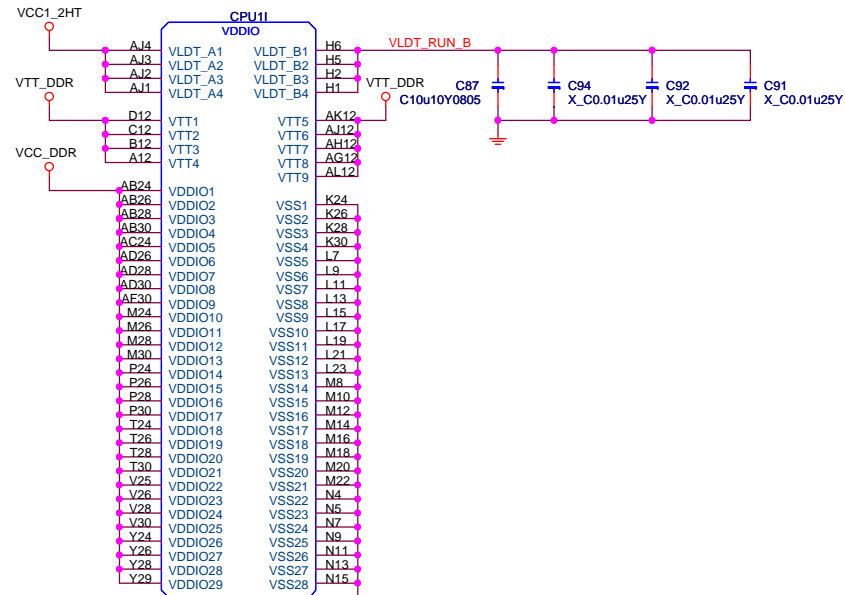
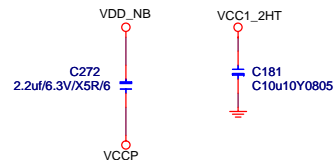
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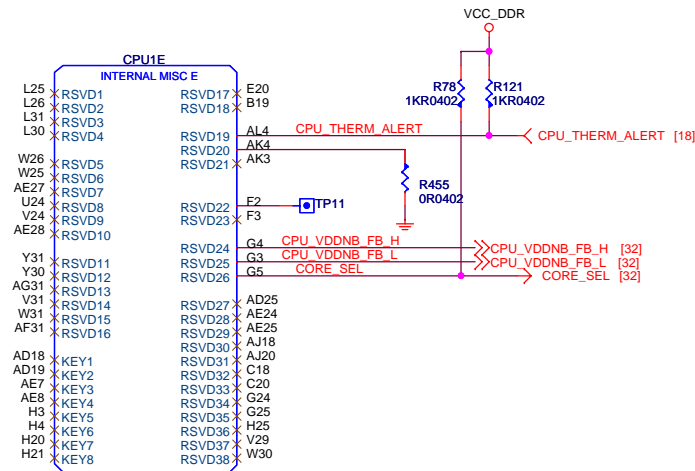
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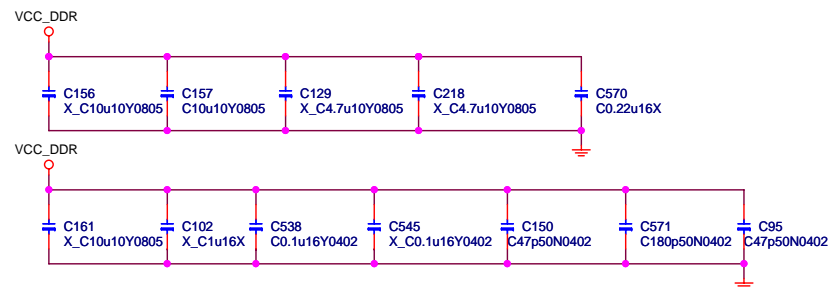
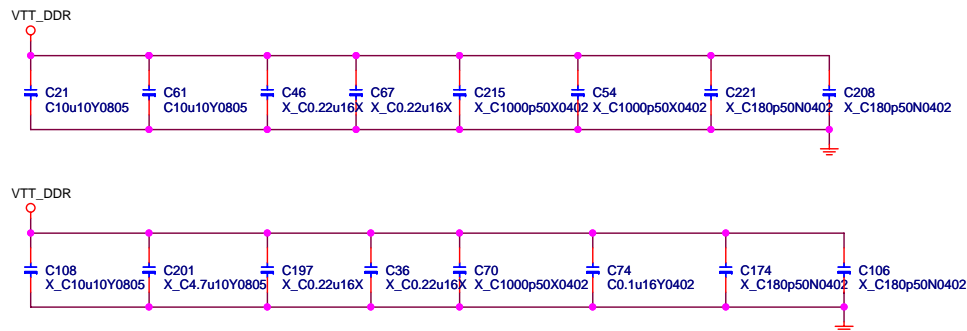


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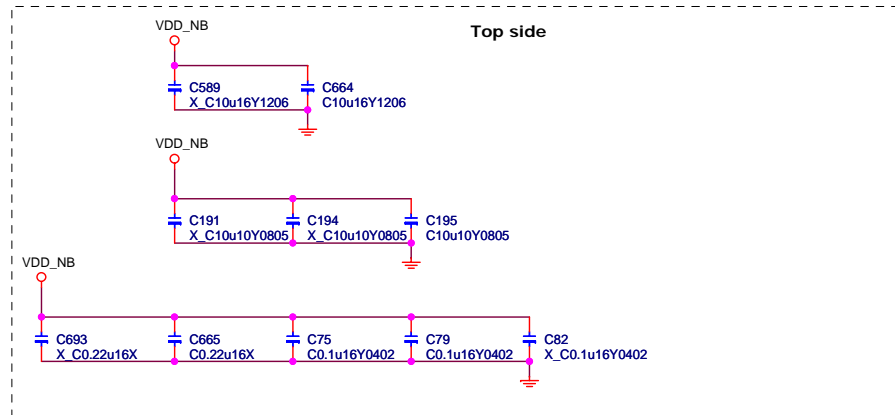
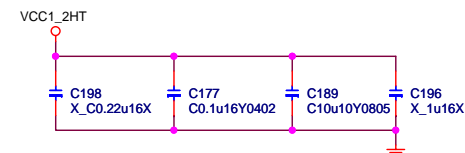
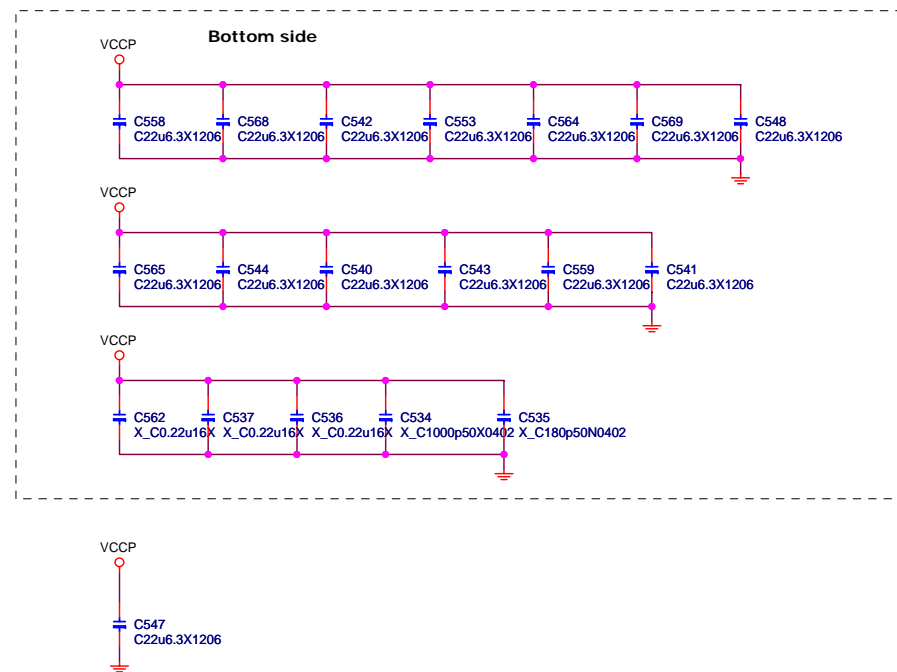
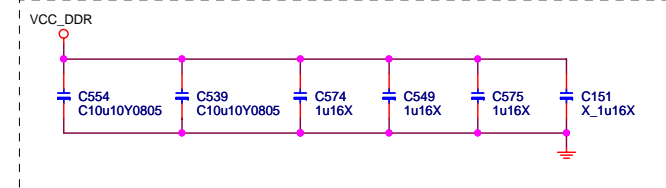


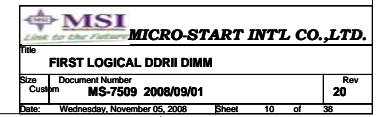
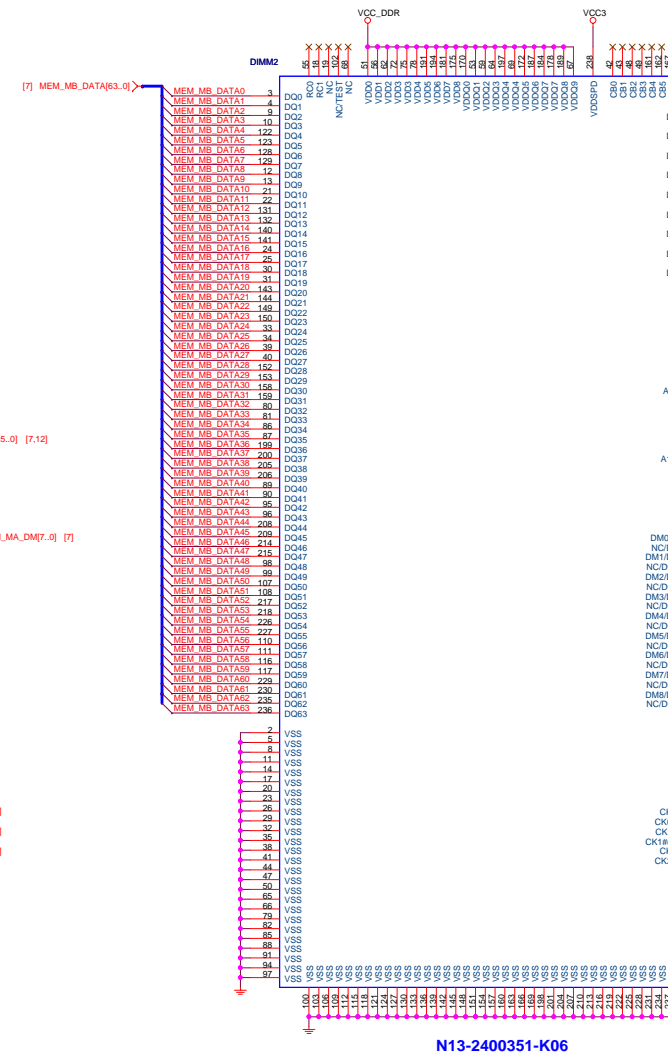
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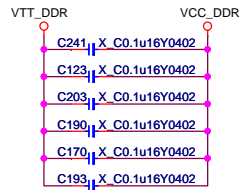
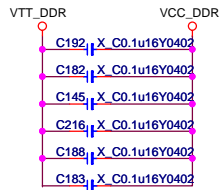
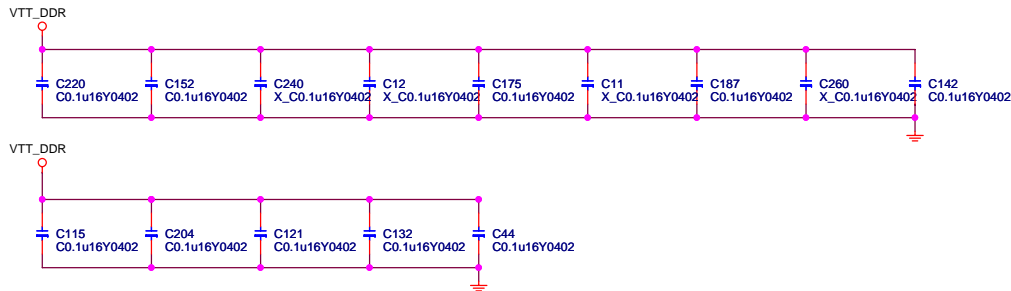
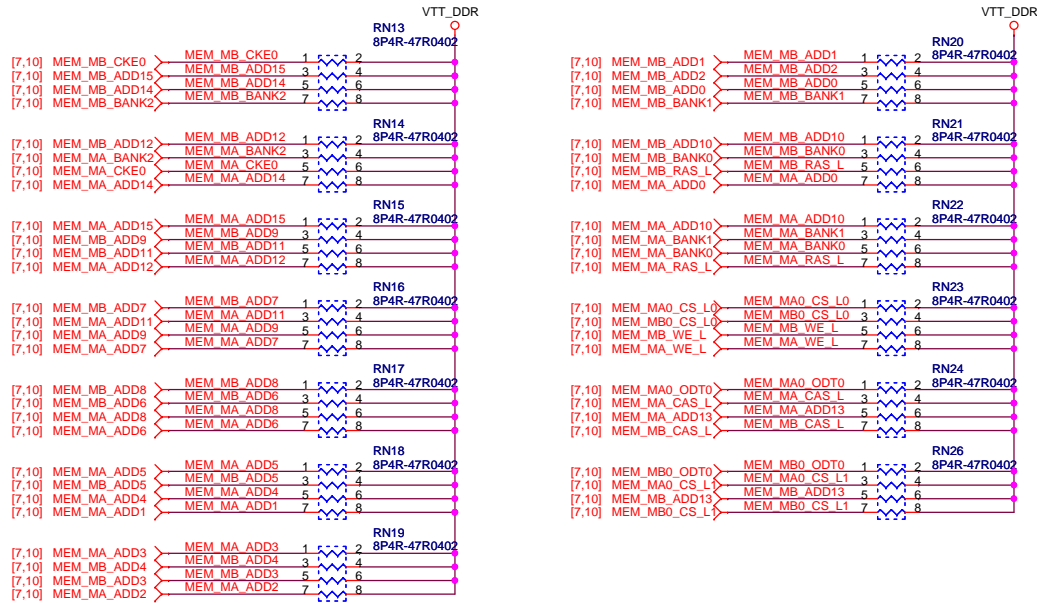


Bottom side

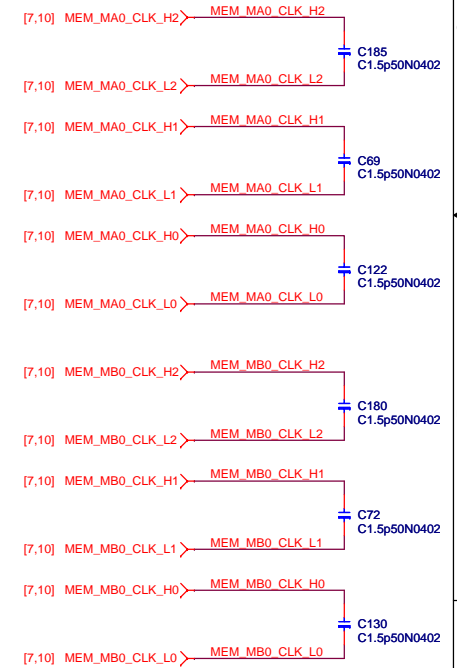
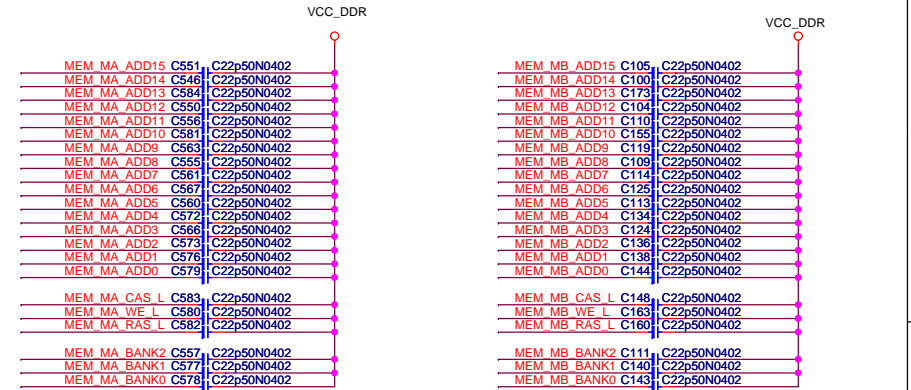




RTT:Place Behind DIMMs



Place Between Processor and DIMMs



MCP68 HyperTransport Receive

Connect directly to CPU HT Transmit Data Bus

CADOP[0..7] P/I N CADOP[8..15] P/I N

CTLOP 0 P/I N CTLOP 1 P/I N

CLKOP0 P/I N CLKOP1 P/I N

Breakout (<700 mil):

Route signal at nominal impedance and 1× trace width spacing.

After Breakout:

Route signal at the impedance specified in AMD *Processor Motherboard Design Guide* and 4× trace width spacing to other signals.

Match pairs to 25 mil.

All signal lengths must match to within 60 mil of

Minimum Length: 1" (150ps)

Maximum Length: 12" (1800ps) for trace ≥ 5mil and 8" (1200ps) for trace = 4mil

MCP68 HyperTransport Transmit

Connect directly to CPU HT Transmit Data Bus

CADIP[0..7] P/I N CADIP[8..15] P/I N

CTLIP0 P/I N CTLIP1 P/I N

CLKIP0 P/I N CLKIP1 P/I N

Breakout (<700 mil):

Route signal at nominal impedance and 1× trace width spacing.

After Breakout:

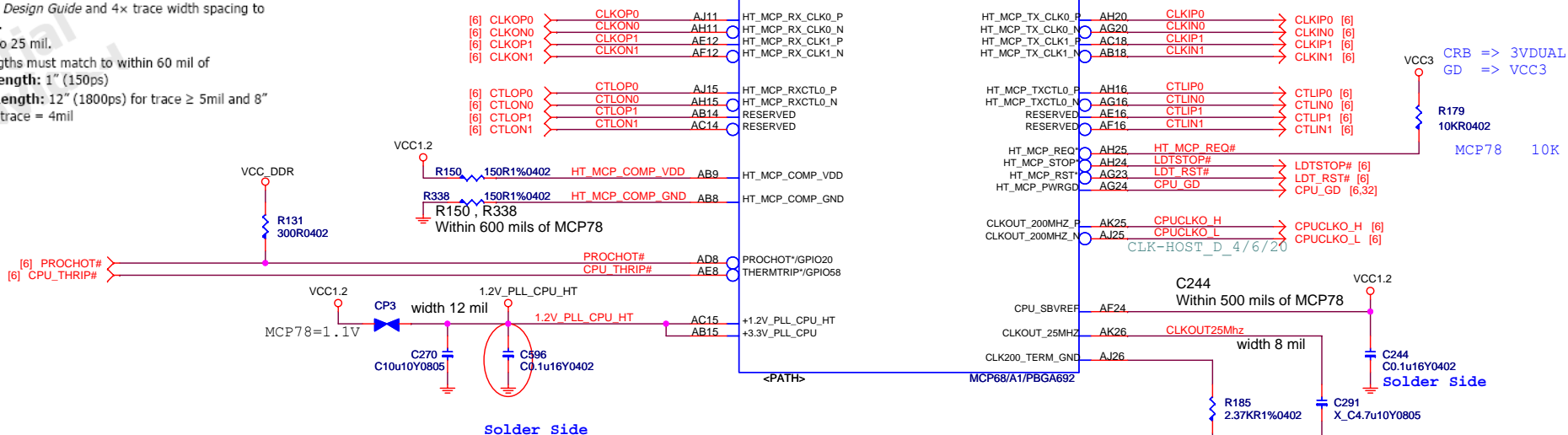
Route signal at the impedance specified in AMD *Processor Motherboard Design Guide* and 4× trace width spacing to other signals.

Match pairs to 25 mil.

All signal lengths must match to within 60 mil of

Minimum Length: 1" (150ps)

Maximum Length: 12" (1800ps) for trace ≥ 5mil and 8" (1200ps) for trace = 4mil



HyperTransport Calibration

HT_MCP_COMP_VDD
HT_MCP_COMP_GND

Breakout (<500 mil):

Route signal at nominal impedance and 1× trace width spacing.

After Breakout:

Route signal at nominal impedance and 2× (or greater) trace width spacing
Maximum Length: 600 mil.

MCP HyperTransport


HT_MCP_REQ# / -LDTSTOP
-LDT_RST / CPU_GD

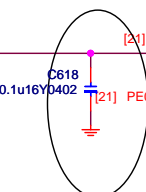
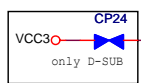
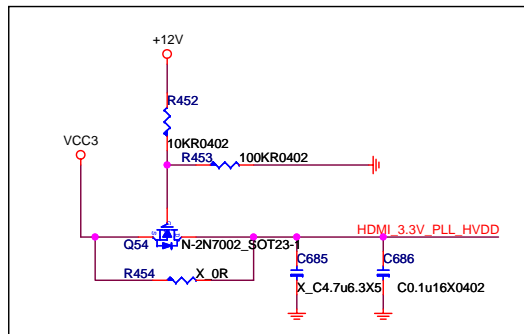
Breakout (<700 mil):

Route signal at nominal impedance and 1× trace width spacing.

After Breakout:

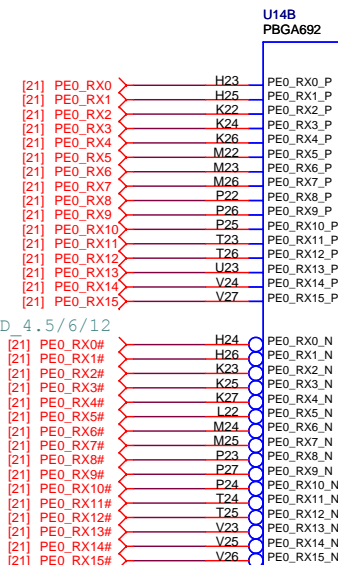
Route signal at nominal impedance and 2× trace width spacing.

| | | |
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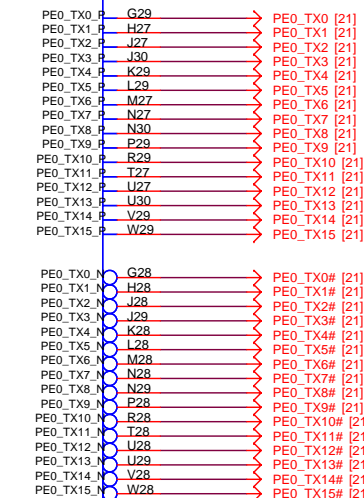


Solder Side

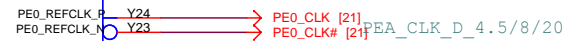
PEx16_D_4.5/6/12



U14B
PBGA692
MCP61
SEC 2 OF 8



PEx16_D_4.5/6/12




Solder Side

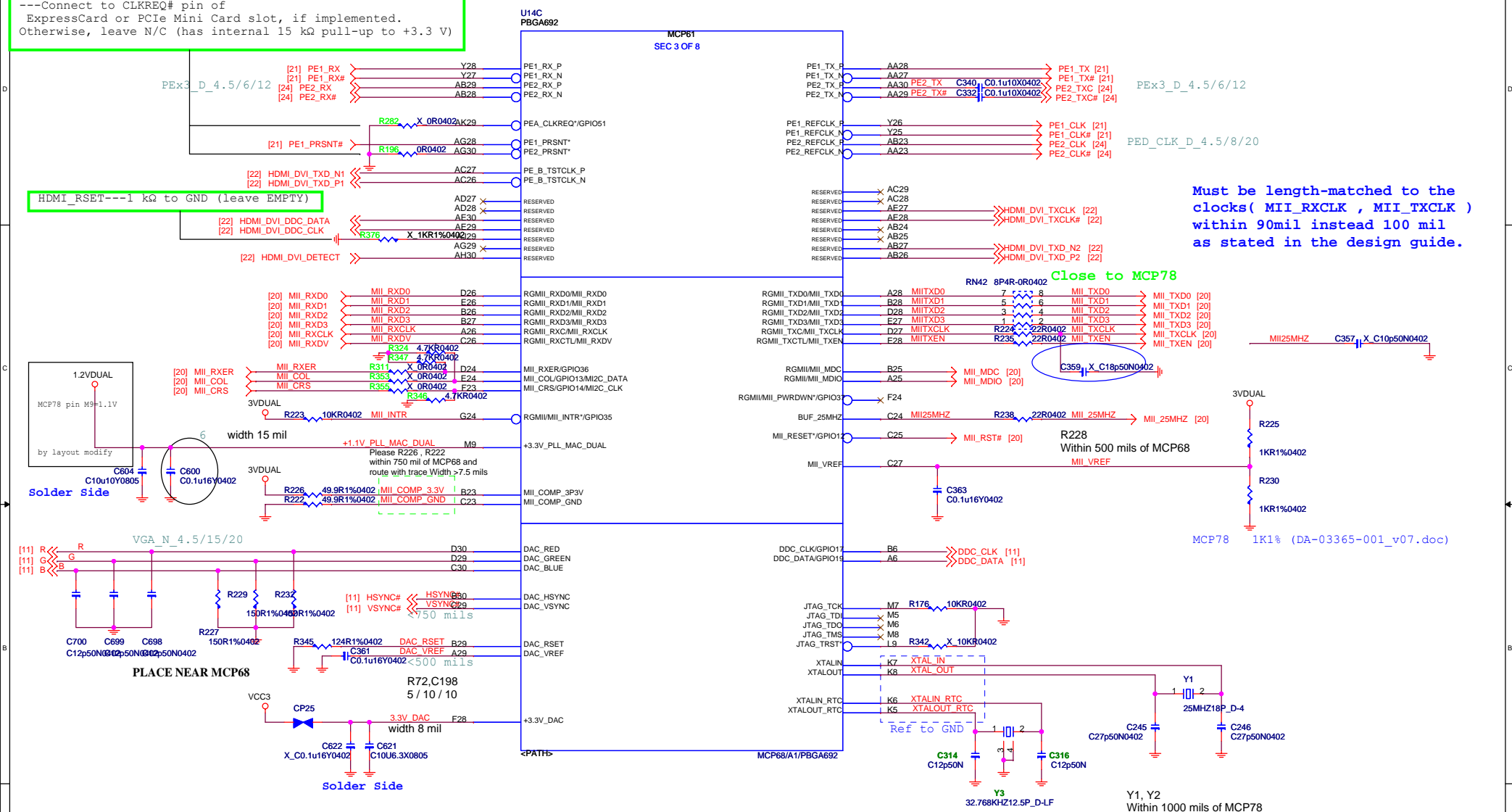
PCI Express Layout Guidelines

The PCI Express differential signal groups are very high speed, running at 2.5 Gbps. Pay special attention to routing these signals.

- Nominal impedance: the differential signal group should be routed at $60\Omega \pm 10\%$ single-ended and $100\Omega \pm 10\%$ differential.
- Maintain 5 mil length matching within each pair, and 20 mil spacing to other pairs and signals, unless otherwise specified.
- Maximum mismatch between pairs is 3,000 mil, and maximum length of any pair is 10,000 mil.
- All traces should be referenced to **GND**.
- There should be no more than four vias per TX trace, and no more than two vias per RX trace on the motherboard.

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```
PEB_PRSN#
---If used with on-board PCIe device,
PRSN# must be connected to GND
PEA_CLKREQ#
---Connect to CLKREQ# pin of
ExpressCard or PCIe Mini Card slot, if implemented.
Otherwise, leave N/C (has internal 15 kΩ pull-up to +3.3 V)
```



RGMII Routing Guidelines


- ❑ All RGMII traces should be referenced to an uncut **GND** or **PWR** plane.
- ❑ Route RGMII traces at $50\ \Omega \pm 10\%$ single-ended to the external PHY.
- ❑ Keep RGMII signal trace lengths to less than 15 inches.
- ❑ Add a 10 k Ω pull-down resistor on any unused input or I/O signal on this interface if it is not connected to a PHY.
- ❑ For reference, differential pair signals from the RGMII PHY to the Ethernet connector should be routed at 55 Ω single-ended/100 Ω differential and 20+ mil spacing from other signals. Match lengths within 25 mil and do not exceed 2 inches in length. Follow vendor recommendations, especially regarding termination and placement.

The parallel capacitors' values for crystal oscillator should be selected to meet the particular crystal manufacturer's C_L requirement. The formula for C_L is usually as follows:

$$C_L = C_S + \frac{(C_0 \times C_1)}{(C_0 + C_1)}$$

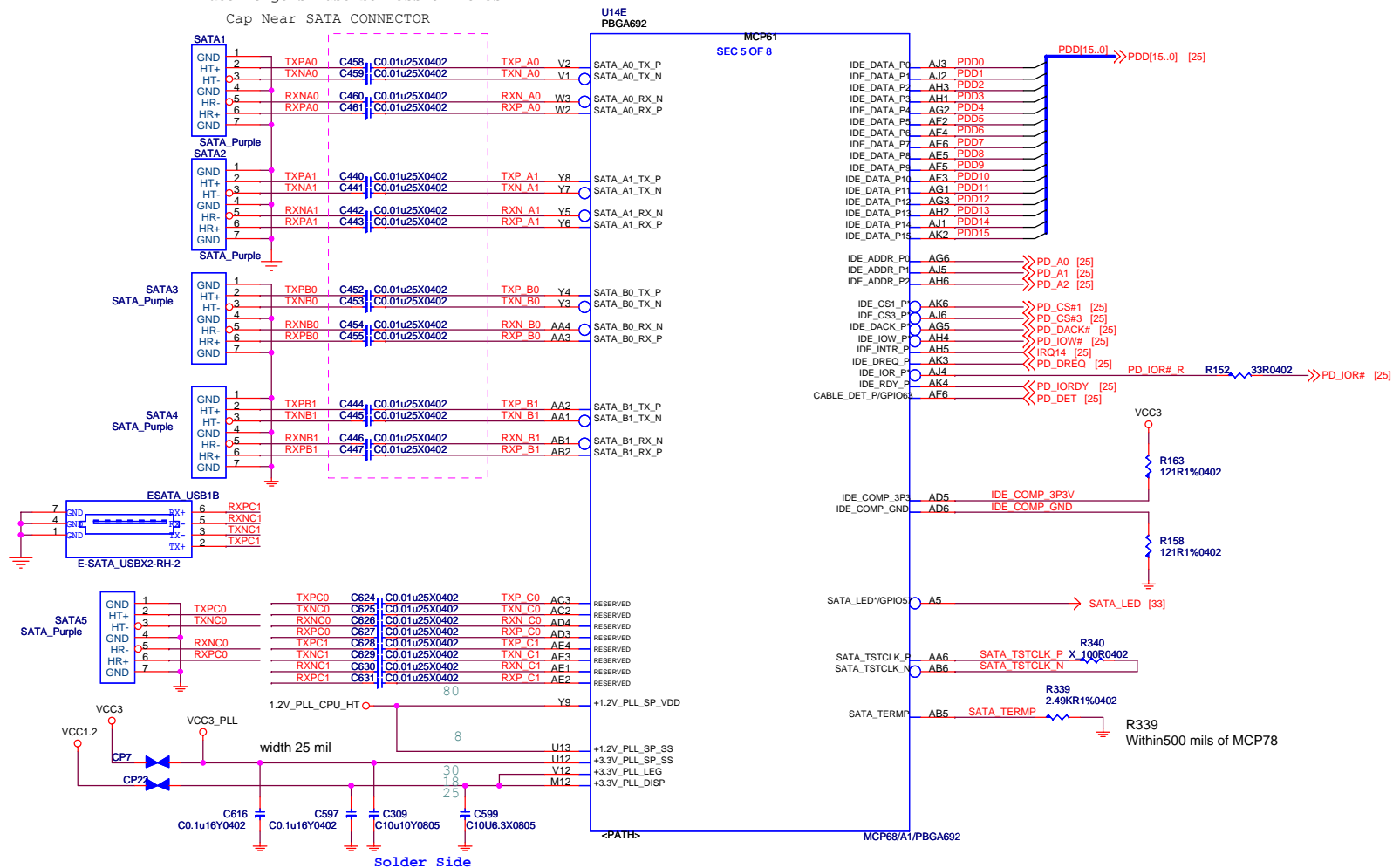
Where:

C_L = Load Capacitance (specified by crystal manufacturer)
 C_S = Stray Capacitance (~ 5 pF)
 C_0 and C_1 = Parallel Capacitance

| | | | | | | | |
|---|--|---|--|-----------------------------------|--|-------------------------|--|
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| Title MCP6B-PEX & MII & DAC | | | | | | | |
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Trace lengths must be less 8 inches

Cap Near SATA CONNECTOR

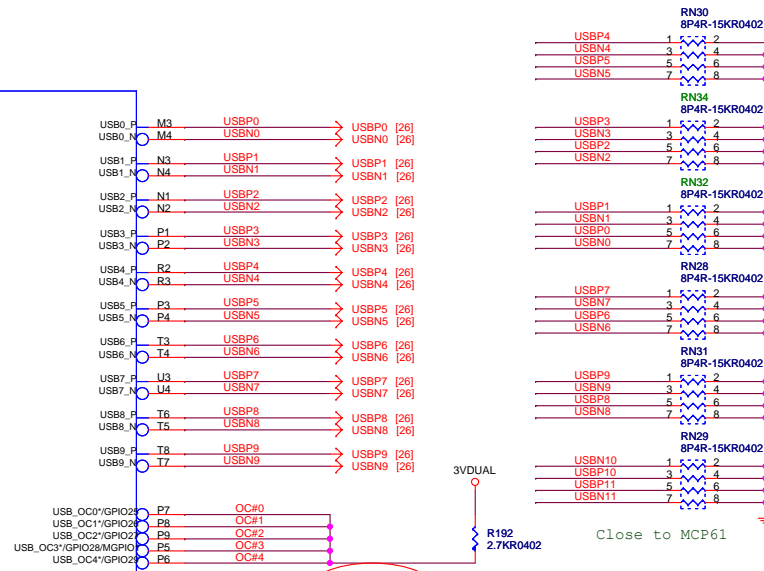


Single-Ended Impedance

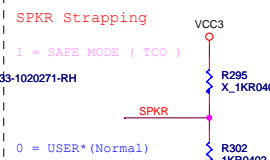
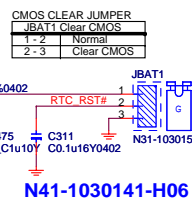
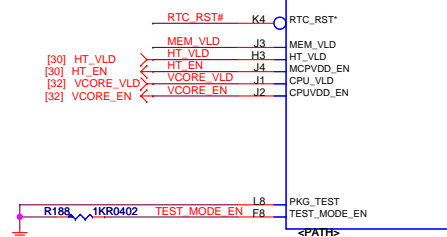
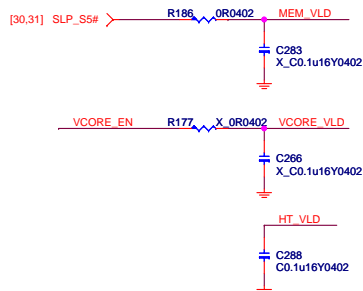
| Trace Width (Based on 4-Layer Stackup) | Impedance | Interfaces |
|---|-----------------------|----------------------|
| 5 mil | 60 Ω \pm 10% | All other interfaces |
| 7 mil | 50 Ω \pm 10% | RGMI, SATA |
| 7.5 mil | 45 Ω \pm 10% | USB |

Differential Impedance

| Trace Width (4-Layer Stackup) | Trace Spacing (4-Layer Stackup) | Impedance | Interfaces |
|----------------------------------|------------------------------------|------------------------|----------------|
| 5 mil | 5 mil | 93 Ω \pm 10% | HyperTransport |
| 5 mil | 6 mil | 100 Ω \pm 10% | PCI Express |
| 7 mil | 12 mil | 100 Ω \pm 10% | SATA |
| 7.5 mil | 7.5 mil | 90 Ω \pm 10% | USB |



POWER SEQUENCE



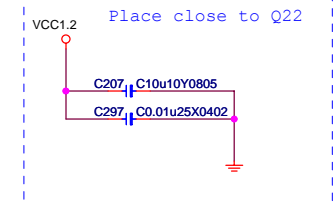
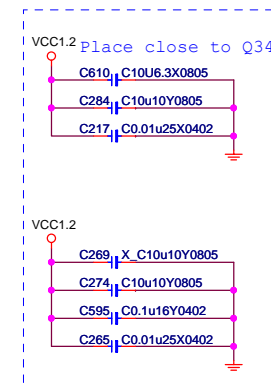
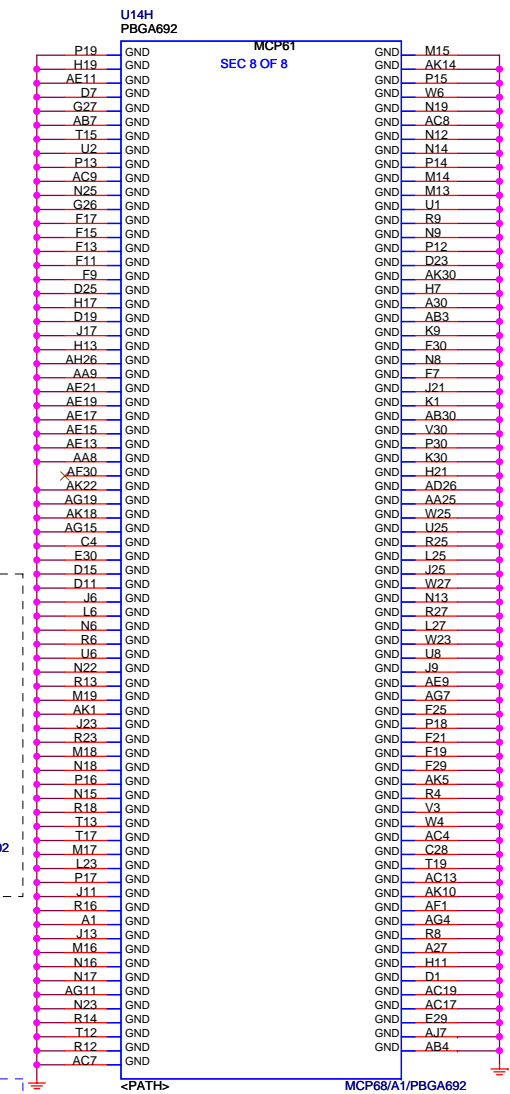
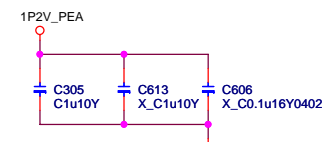
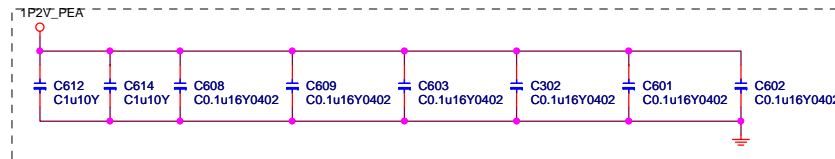
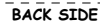
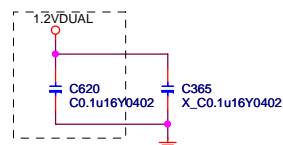
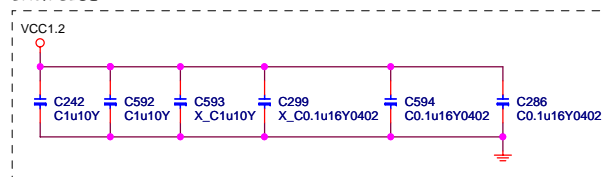
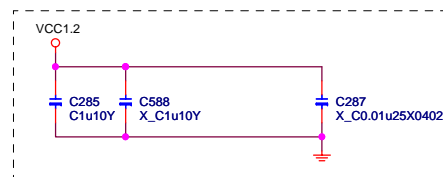
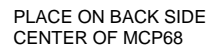
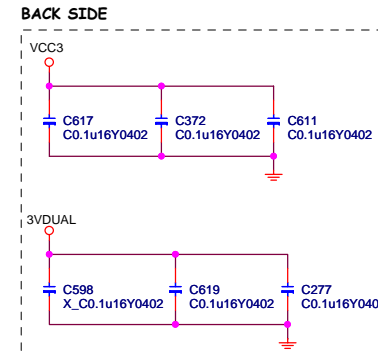
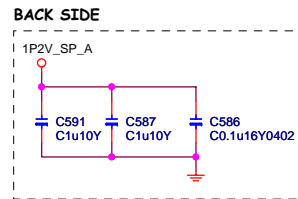
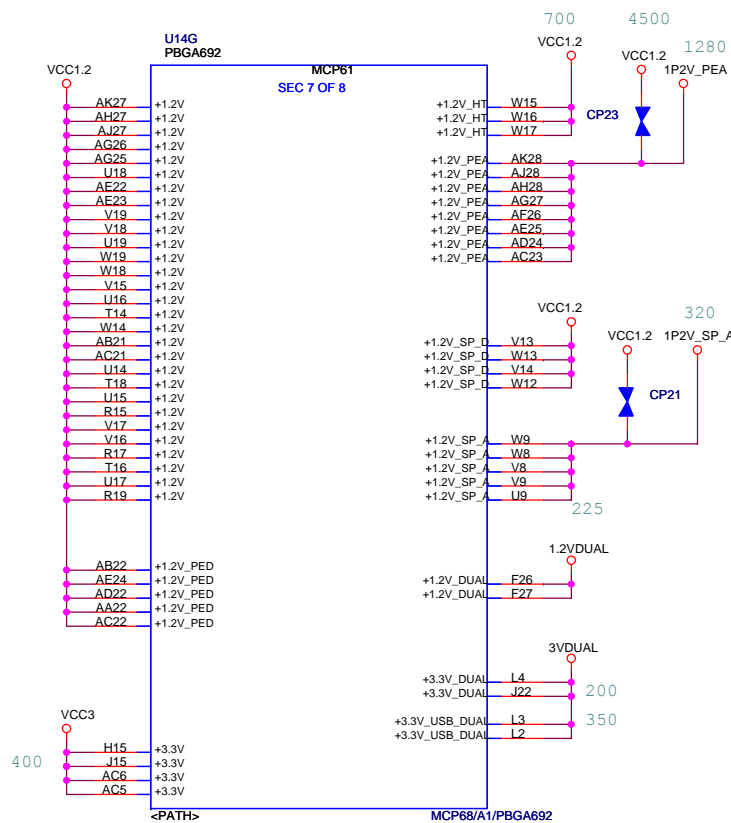
SPKR

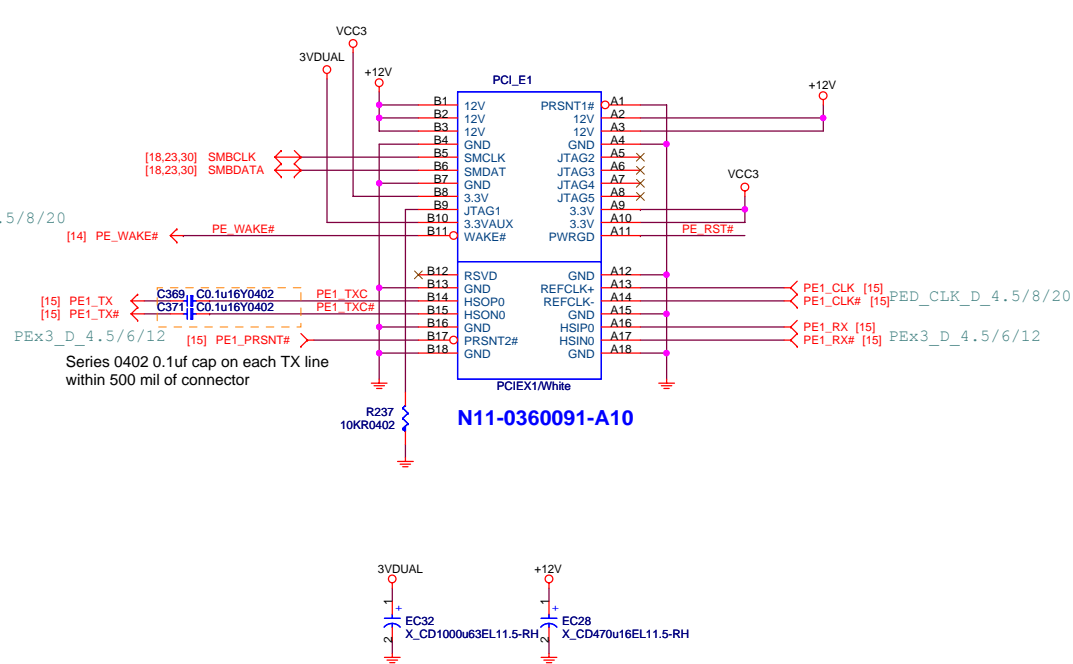
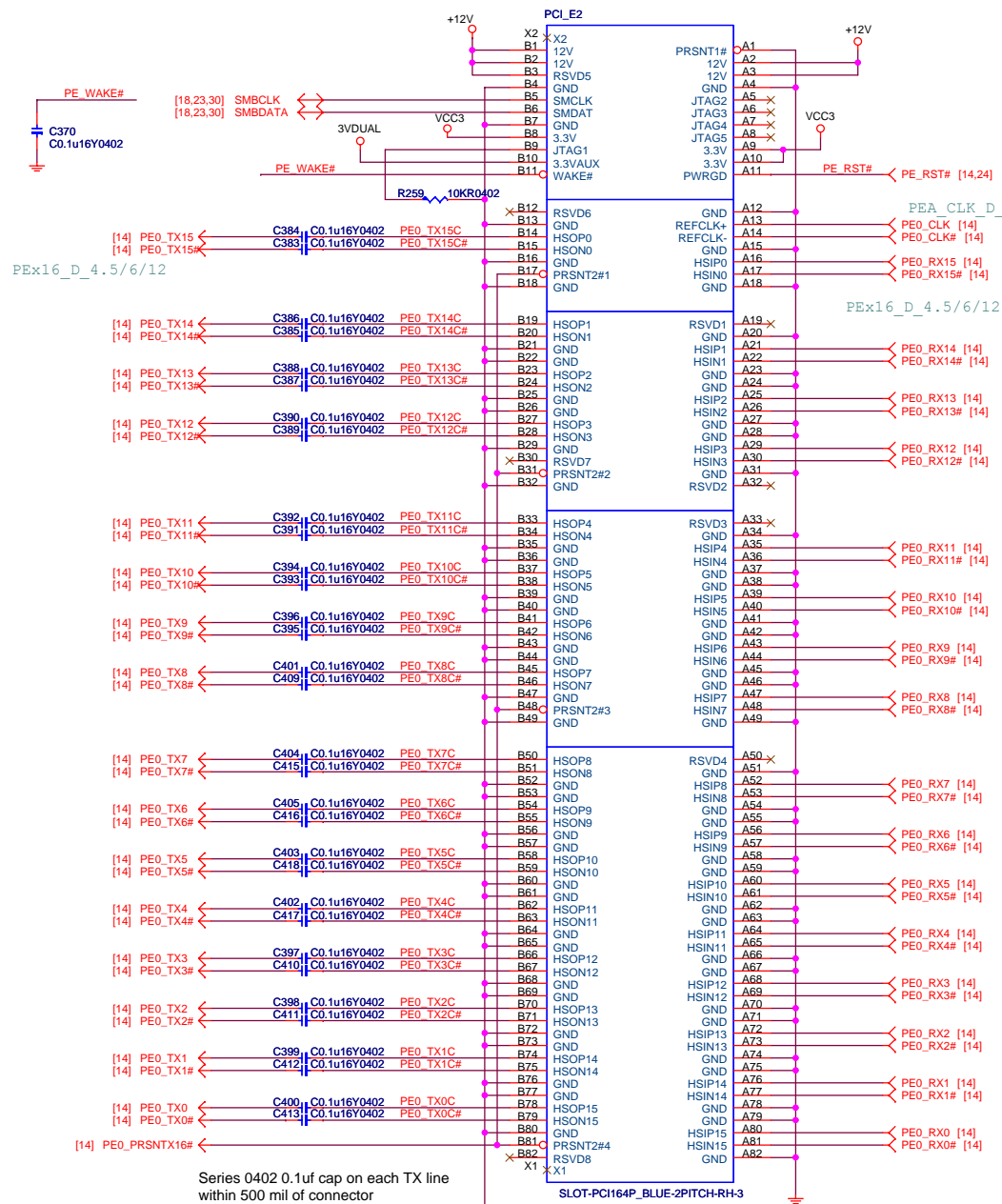
Boot mode
select

: User Mode Boot Init table (TCO timer enabled)
 : Safe Mode Boot Init table (TCO timer disabled)

Selects between a USER table and a SAFE table for boot initialization parameters.

Note: When booting the SAFE table, it is assumed that the boot values are valid, so the automatic recovery logic is disabled (TCO timer does not reboot the system).



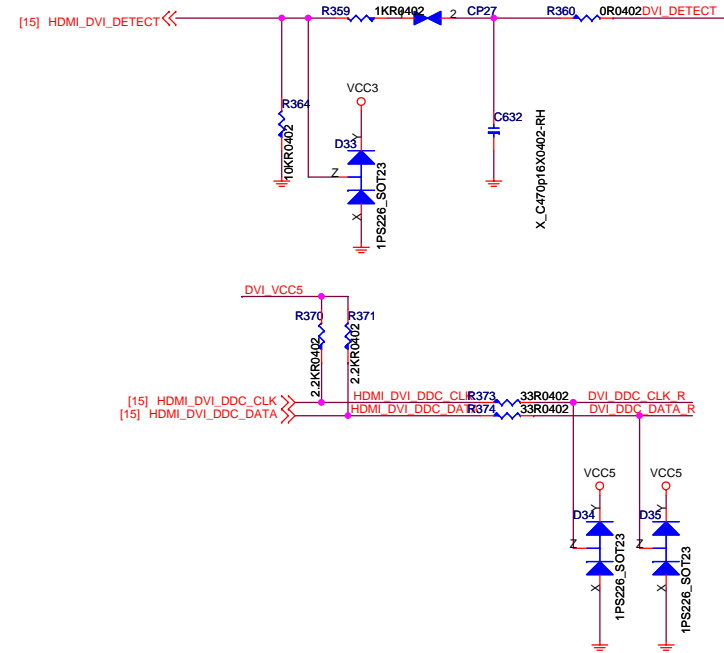
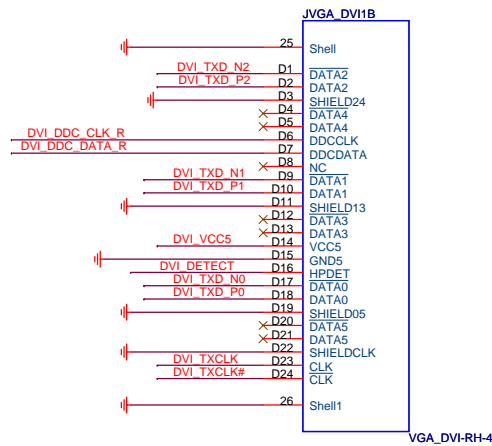
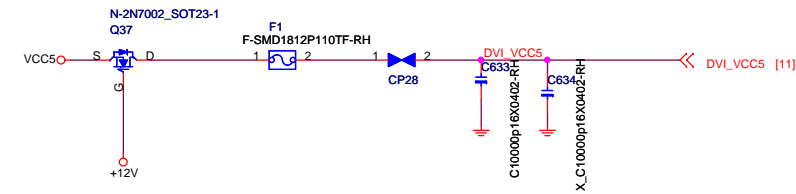
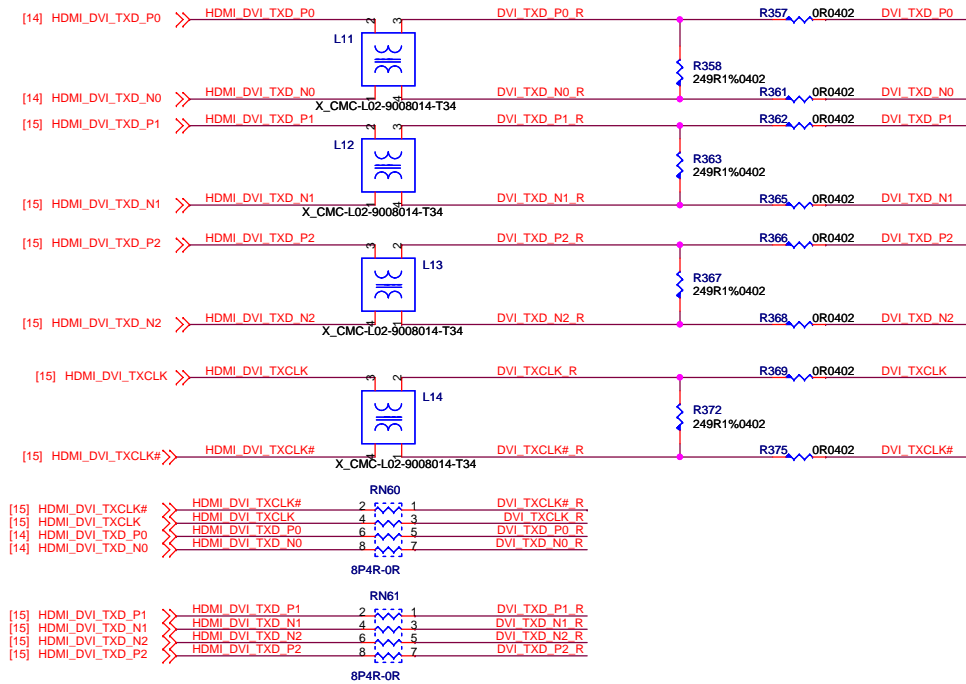


PCI Express Layout Guidelines

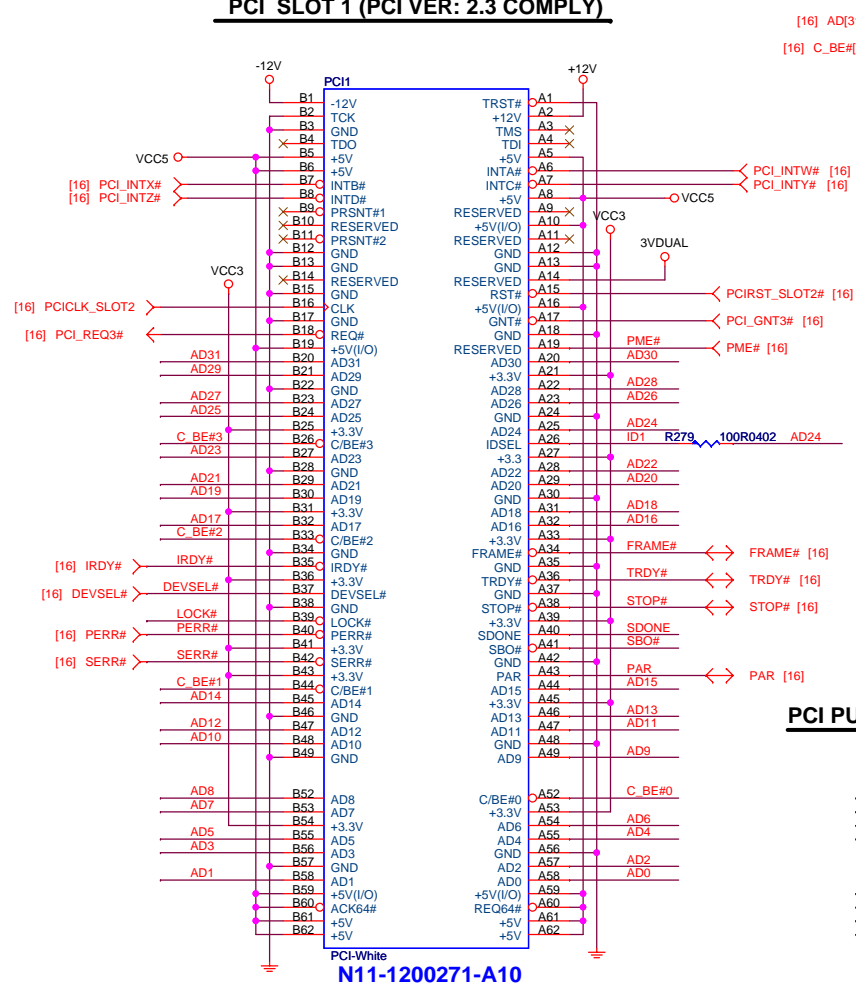
The PCI Express differential signal groups are very high speed, running at 2.5 Gbps. Pay special attention to routing these signals.

- Nominal impedance: the differential signal group should be routed at $60\Omega \pm 10\%$ single-ended and $100\Omega \pm 10\%$ differential.
- Maintain 5 mil length matching within each pair, and 20 mil spacing to other pairs and signals, unless otherwise specified.
- Maximum mismatch between pairs is 3,000 mil, and maximum length of any pair is 10,000 mil.
- All traces should be referenced to GND.
- There should be no more than four vias per TX trace, and no more than two vias per RX trace on the motherboard.

for EMI place near DVI connector



PCI SLOT 1 (PCI VER: 2.3 COMPLY)



N11-1200271-A10

MCP78V

IDSEL = AD24

PCI_REQ3# PCI_GNT3#

PCI_INTW#

Device # 8

MCP61 IDSEL, INT, and REQ/GNT

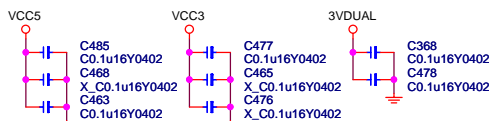
| Slot | IDSEL | Slot INTA# | Slot INTB# | Slot INTC# | Slot INTD# | REQ/GNT | Device # |
|------|----------|------------|------------|------------|------------|---------|----------|
| 1 | PCI_AD26 | INTY# | INTZ# | INTW# | INTX# | 4 | 9 |
| 2 | PCI_AD25 | INTY# | INTZ# | INTW# | INTX# | 3 | 8 |
| 3 | PCI_AD24 | INTW# | INTX# | INTY# | INTZ# | 2 | 7 |
| 4 | PCI_AD23 | INTZ# | INTW# | INTX# | INTY# | 1 | 6 |
| 5 | PCI_AD22 | INTY# | INTZ# | INTW# | INTX# | 0 | 5 |

| | |
|-------|-------------------------|
| MCP68 | IDSEL, INT, and REQ/GNT |
|-------|-------------------------|

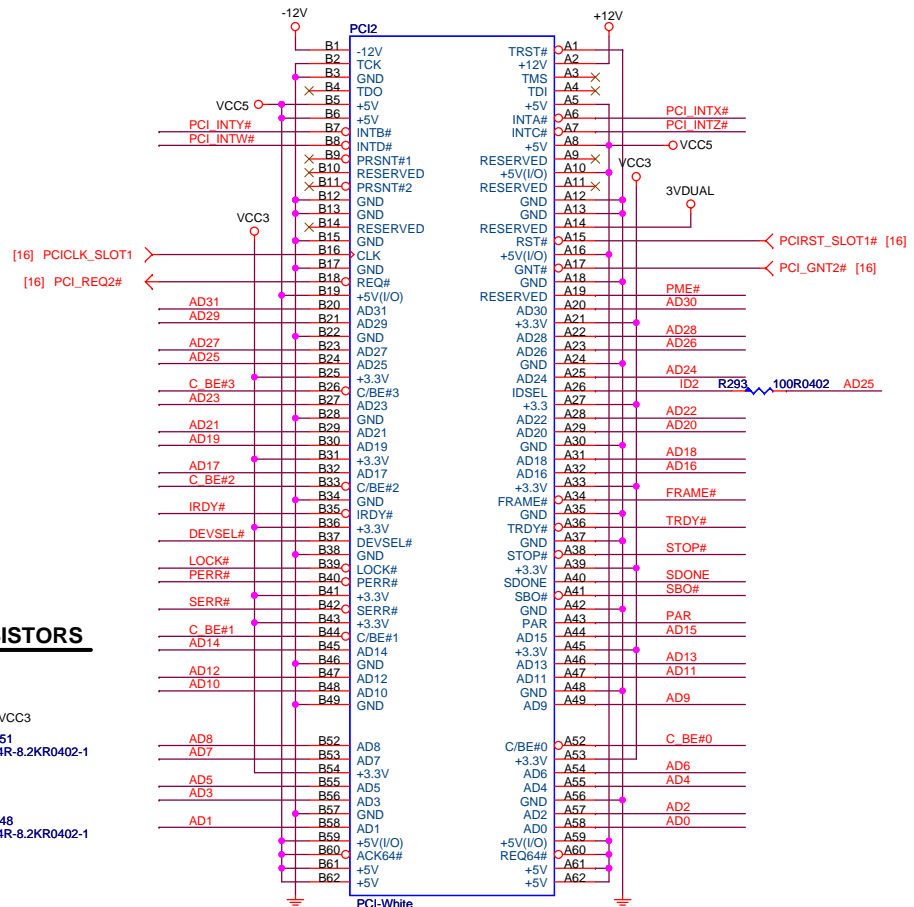
| Slot | IDSEL | Slot INTA# | Slot INTB# |
|------|----------|------------|------------|
| 1 | PCI_A025 | INTX# | INTY# |
| 2 | PCI_A024 | INTW# | INTX# |
| 3 | PCI_A023 | INTZ# | INTW# |
| 4 | PCI_A022 | INTY# | INTZ# |
| 5 | PCI_A021 | INTX# | INTY# |

| REQ/GNT | Device # |
|---------|----------|
| 4 | 9 |
| 3 | 8 |
| 2 | 7 |
| 1 | 6 |
| 0 | 5 |

PCI SLOT DECOUPLING CAPACITORS



PCI SLOT 2 (PCI VER: 2.3 COMPLY)



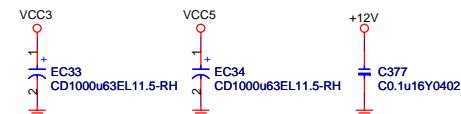
N11-1200271-A10

MCP78V

IDSEL = AD25

PCI_REQ2# PCI_GNT2#

PCI_INTX#

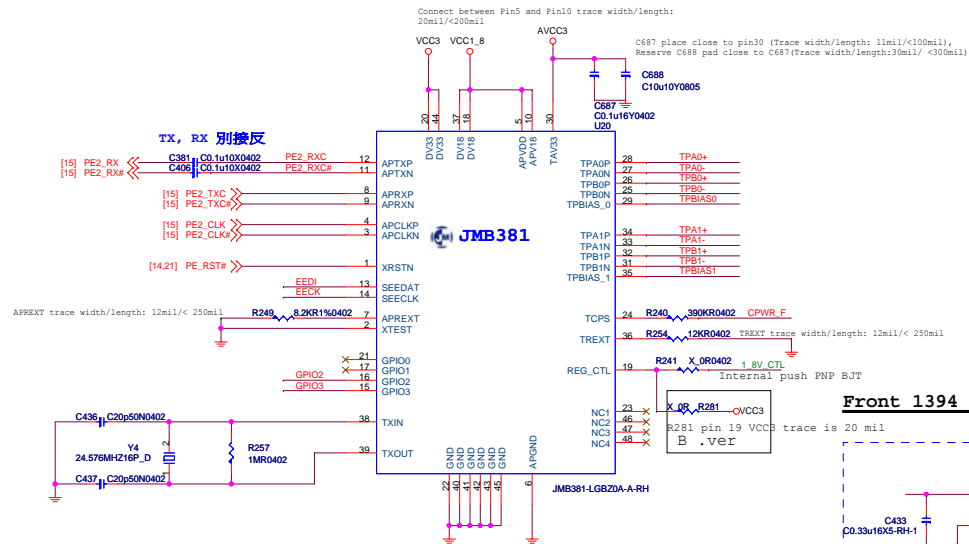
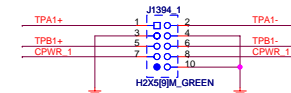
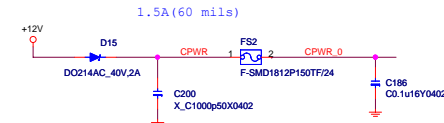
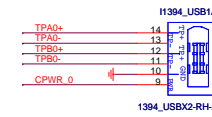
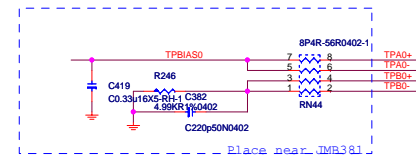
Device # 9

| | |
|-------|--------------|
| Title | PCI SLOT 1&2 |
|-------|--------------|

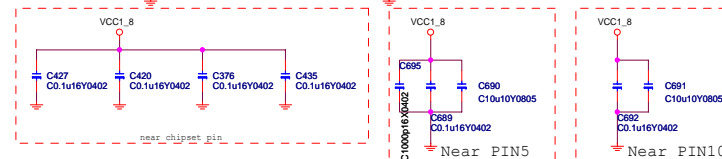
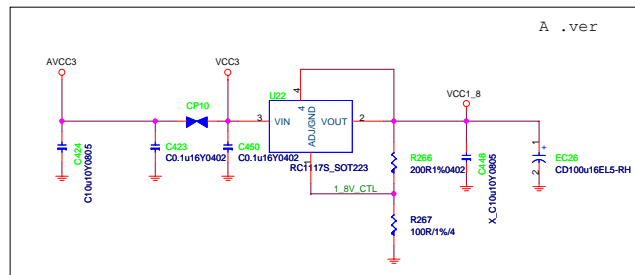
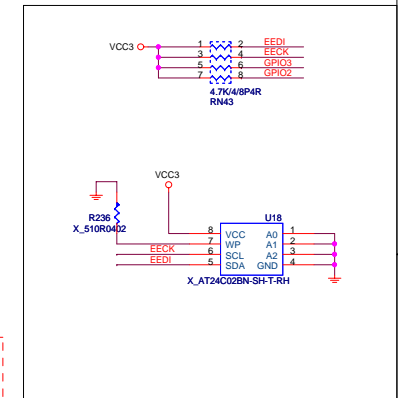
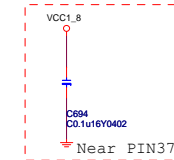
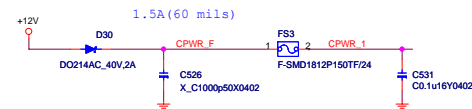
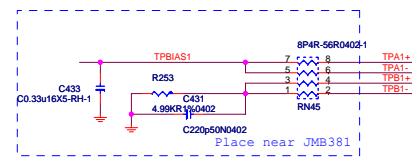
| | |
|--------|---------------------------|
| Size | Document Number |
| Custom | MS-7509 2008/09/01 |

Date: Wednesday, November 05, 2008 Sheet 23 of 38

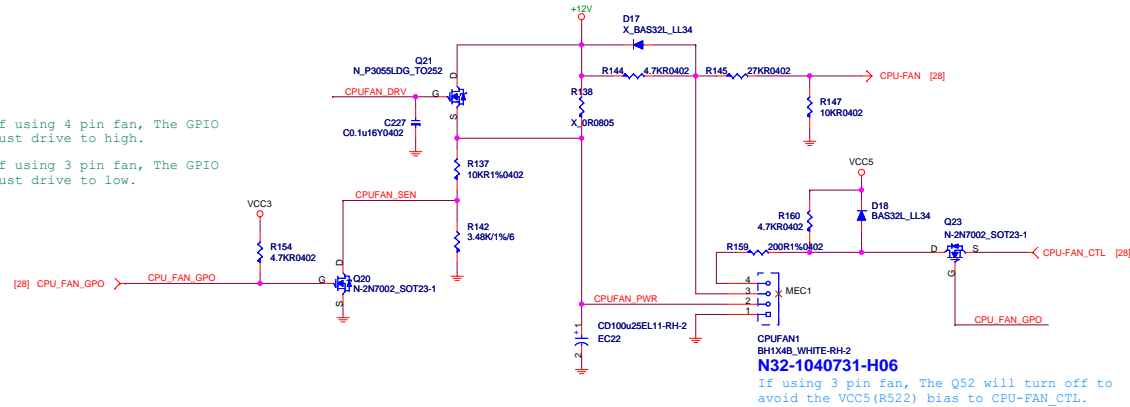
1394 CONTROLLER

Rear 1394 port

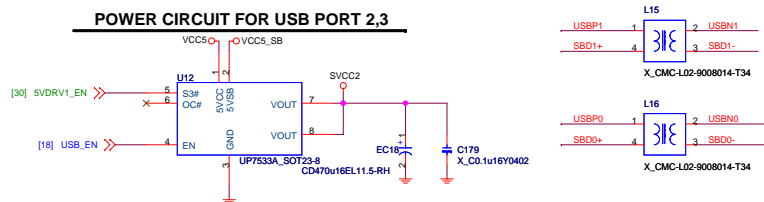
Front 1394 pin header



Pin configuration diagram for the X510R0402 component. The diagram shows a central component with pins numbered 1 to 40. Pin 1 is connected to VCC5. Pin 2 is connected to PDD[15..0]. Pin 3 is connected to HD_RST#. Pin 4 is connected to PDD7. Pin 5 is connected to PDD6. Pin 6 is connected to PDD5. Pin 7 is connected to PDD4. Pin 8 is connected to PDD3. Pin 9 is connected to PDD2. Pin 10 is connected to PDD1. Pin 11 is connected to PDD0. Pin 12 is connected to PDD15. Pin 13 is connected to PDD14. Pin 14 is connected to PDD13. Pin 15 is connected to PDD12. Pin 16 is connected to PDD11. Pin 17 is connected to PDD10. Pin 18 is connected to PDD9. Pin 19 is connected to PDD8. Pin 20 is connected to PDD7. Pin 21 is connected to PDD6. Pin 22 is connected to PDD5. Pin 23 is connected to PDD4. Pin 24 is connected to PDD3. Pin 25 is connected to PDD2. Pin 26 is connected to PDD1. Pin 27 is connected to PDD0. Pin 28 is connected to PDD15. Pin 29 is connected to PDD14. Pin 30 is connected to PDD13. Pin 31 is connected to PDD12. Pin 32 is connected to PDD11. Pin 33 is connected to PDD10. Pin 34 is connected to PDD9. Pin 35 is connected to PDD8. Pin 36 is connected to PDD7. Pin 37 is connected to PDD6. Pin 38 is connected to PDD5. Pin 39 is connected to PDD4. Pin 40 is connected to PDD3. The diagram also shows connections for VCC3, R156, X_8.2KR0402, and IRQ14.

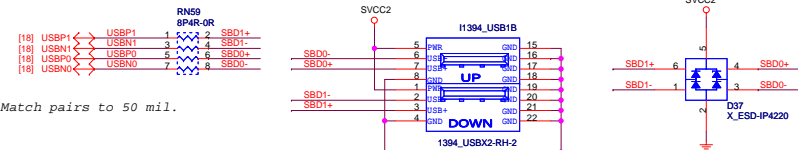
CPU FAN
55555[illegible]

POWER CIRCUIT FOR USB PORT 2,3



REAR PANEL USB CONNECTOR FOR USB PORT 0,1

Trace lengths must be less 12 inches

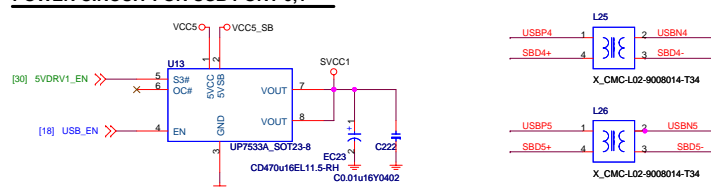


Match pairs to 50 mil.

NEAR USB CONNECTOR

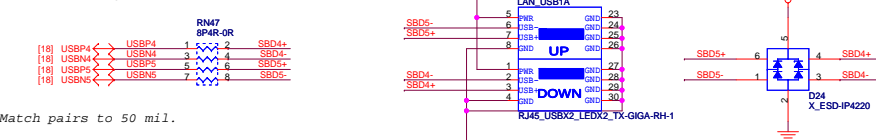
22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

POWER CIRCUIT FOR USB PORT 0,1



FRONT PANEL USB CONNECTOR FOR USB PORT 4,5

Trace lengths must be less 5 inches

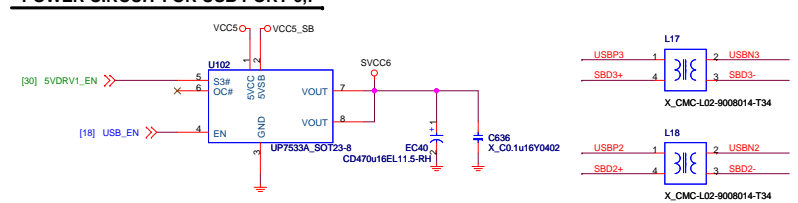


Match pairs to 50 mil.

NEAR USB CONNECTOR

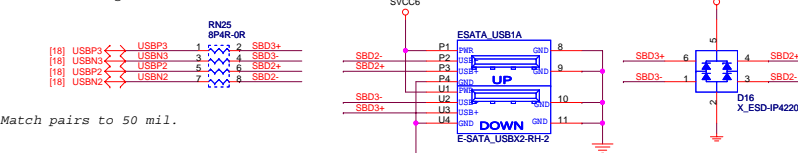
22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

POWER CIRCUIT FOR USB PORT 6,7



REAR PANEL USB CONNECTOR FOR USB PORT 2,3

Trace lengths must be less 12 inches



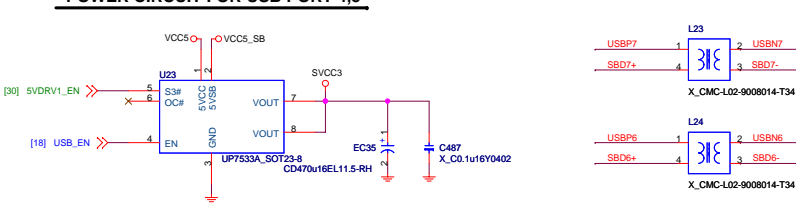
Match pairs to 50 mil.

N58-22F0181-S42

NEAR USB CONNECTOR

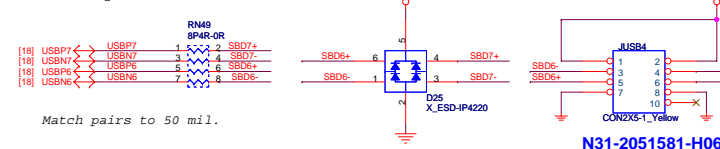
22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

POWER CIRCUIT FOR USB PORT 4,5



FRONT PANEL USB CONNECTOR FOR USB PORT 6,7

Trace lengths must be less 5 inches



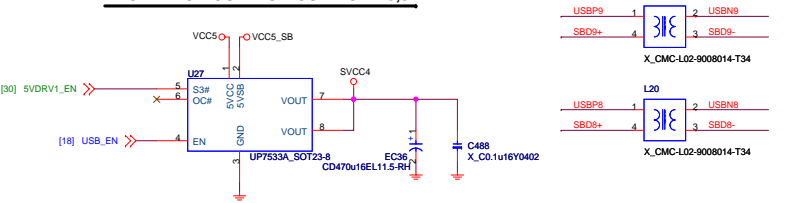
Match pairs to 50 mil.

N31-2051581-H06

NEAR USB CONNECTOR

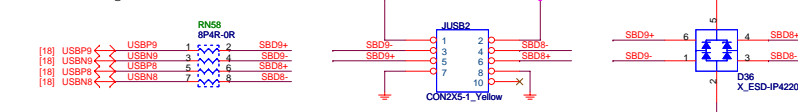
22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

POWER CIRCUIT FOR USB PORT 8,9



FRONT PANEL USB CONNECTOR FOR USB PORT 8,9

Trace lengths must be less 5 inches



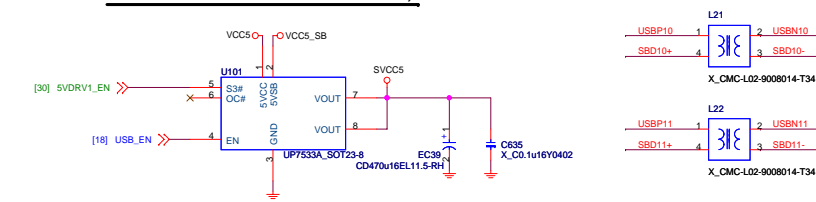
Match pairs to 50 mil.

N31-2051581-H06

NEAR USB CONNECTOR

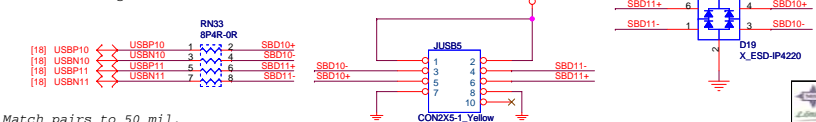
22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

POWER CIRCUIT FOR USB PORT 10,11



REAR PANEL USB CONNECTOR FOR USB PORT 10,11

Trace lengths must be less 5 inches



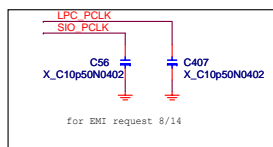
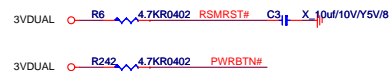
Match pairs to 50 mil.

N31-2051581-H06

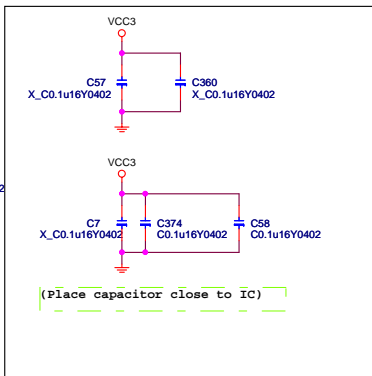
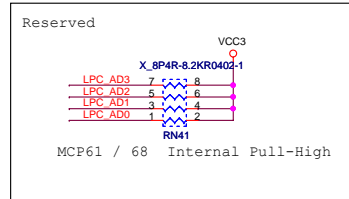
NEAR USB CONNECTOR

22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

LPC length should be less than 18 inches.



Pin 14 connection diagram for X_H2X710JM-2PITCH_1_BLACK-RH. The diagram shows a 14-pin connector with pins 1 through 14. Pin 1 is connected to LPC_PCLK. Pin 2 is connected to JTPM_RST#. Pin 3 is connected to LPC_ADO. Pin 4 is connected to LPC_AD1. Pin 5 is connected to LPC_AD2. Pin 6 is connected to LPC_AD3. Pin 7 is connected to LPC_FRAME#. Pin 8 is connected to JTPM_RST#. Pin 9 is connected to LPC_ADO. Pin 10 is connected to LPC_AD1. Pin 11 is connected to LPC_AD2. Pin 12 is connected to LPC_AD3. Pin 13 is connected to LPC_FRAME#. Pin 14 is connected to JTPM_RST#. The diagram also shows connections to 3VDUAL, VCC3, and VCC5. The bottom label is X_H2X710JM-2PITCH_1_BLACK-RH.



VCCP

R11 10kR1%0402 VIN1

VCC5_SB

R2 200kR1%0402 VIN3

R12 47kR1%0402-RH

VCC5

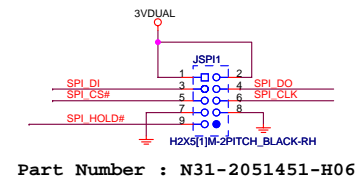
R3 200kR1%0402 VIN4

R13 47kR1%0402-RH

+12V

R4 200kR1%0402 VIN5

R14 20kR0402-2

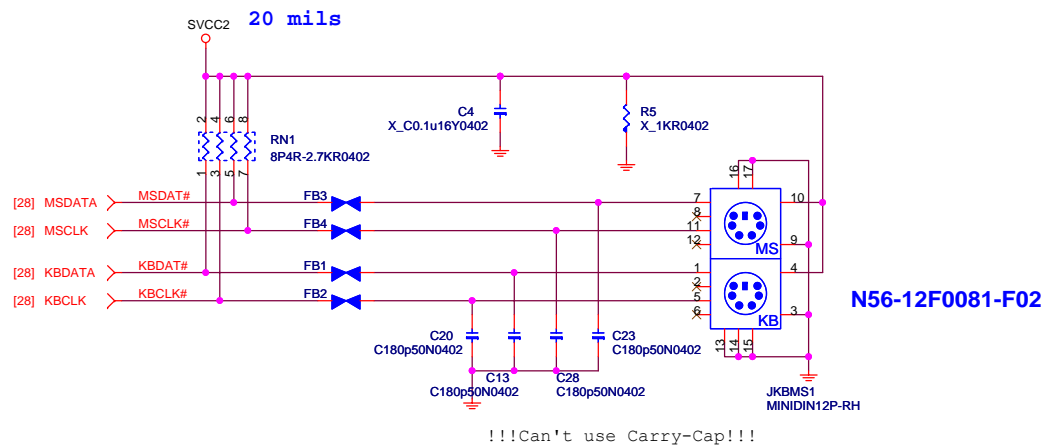


| | | |
|-------|-----|-----------|
| SOUTB | R50 | 1KR0402 |
| SOUTA | R41 | X 1KR0402 |
| RTSA# | R39 | X 1KR0402 |
| RTSB# | R52 | X 1KR0402 |
| DTRB# | R51 | 1KR0402 |
| DTRA# | R34 | X 1KR0402 |

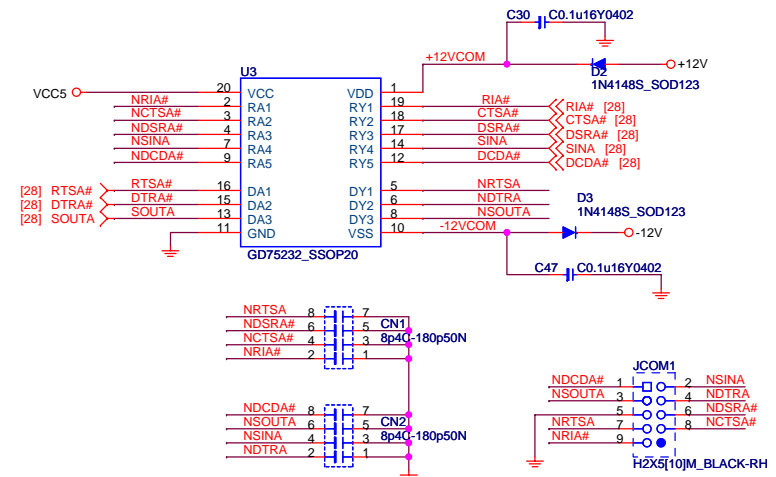
| | Don't STUFF | STUFF |
|-------------|------------------------------------|-------------------------------------|
| DTRB# | SPI as a backup BIOS | SPI as a primary BIOS |
| RTSB# | PWM FAN | LINEAR FAN |
| RTSA# | PIN49-54=VID_OUT PIN42-47=VIDIN | PIN49-54=GPIO PIN42-47=VIDIN/OUT |
| SOUTA | 4E | 2E |
| SOUTB/DTRB# | SPI_DISABLE | SPI_ENABLE |
| DTRA# | FAN START DUTY 60% | FAN START DUTY 100% |

[illegible][illegible]

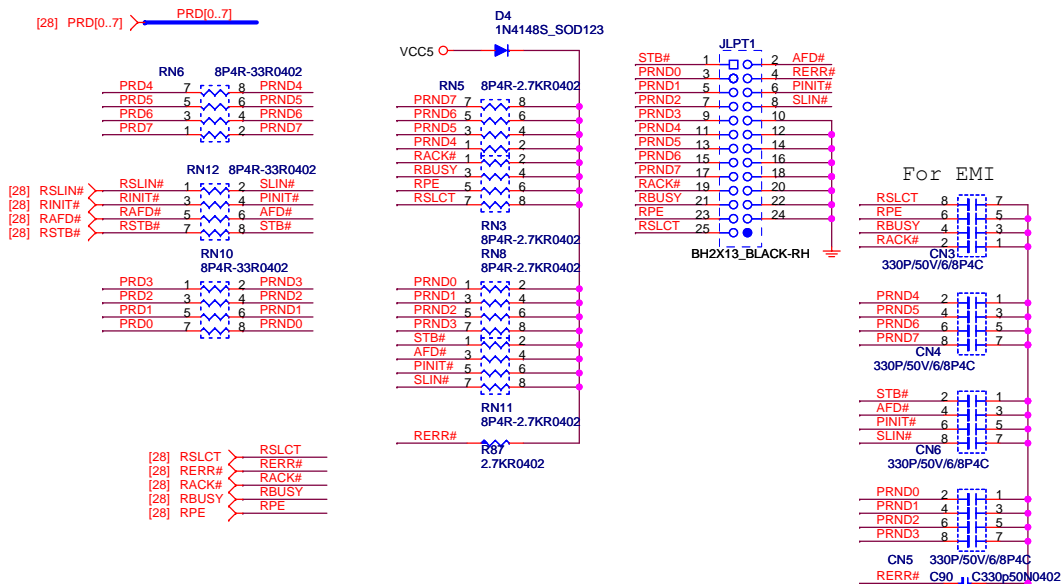
PS2 KEYBOARD & MOUSE CONNECTOR



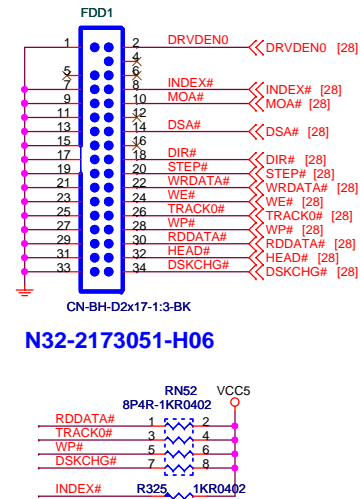
SERIAL PORT 1



PARALLAL PORT



FLOPPY CONN BOLCK



$$V_o \cdot I_o = P = V_i \cdot I_i$$
$$33.509A \cdot 1.8V = 60.31W$$

$$EC: 2.35 \times 3 \times 1.7 = 11.985A$$

33.509A

VCC_DDR

CONNECT TO CHOKE OUTPUT

C131 X_C47p50N0402

C141 X_C47p50N0402

C137 X_C68p50N0402-RH

C96 C68p50N0402-RH

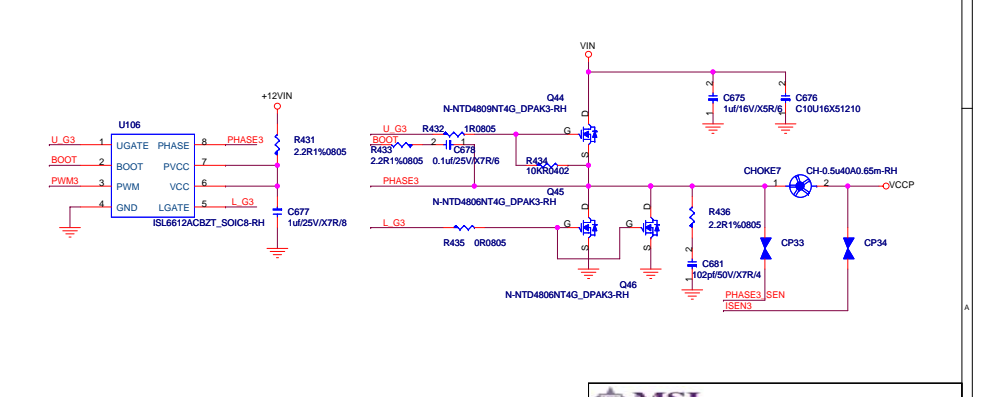
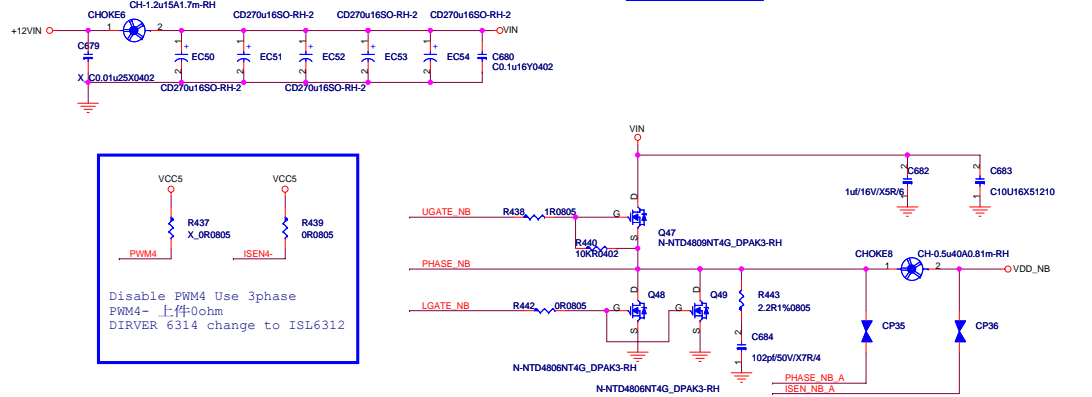
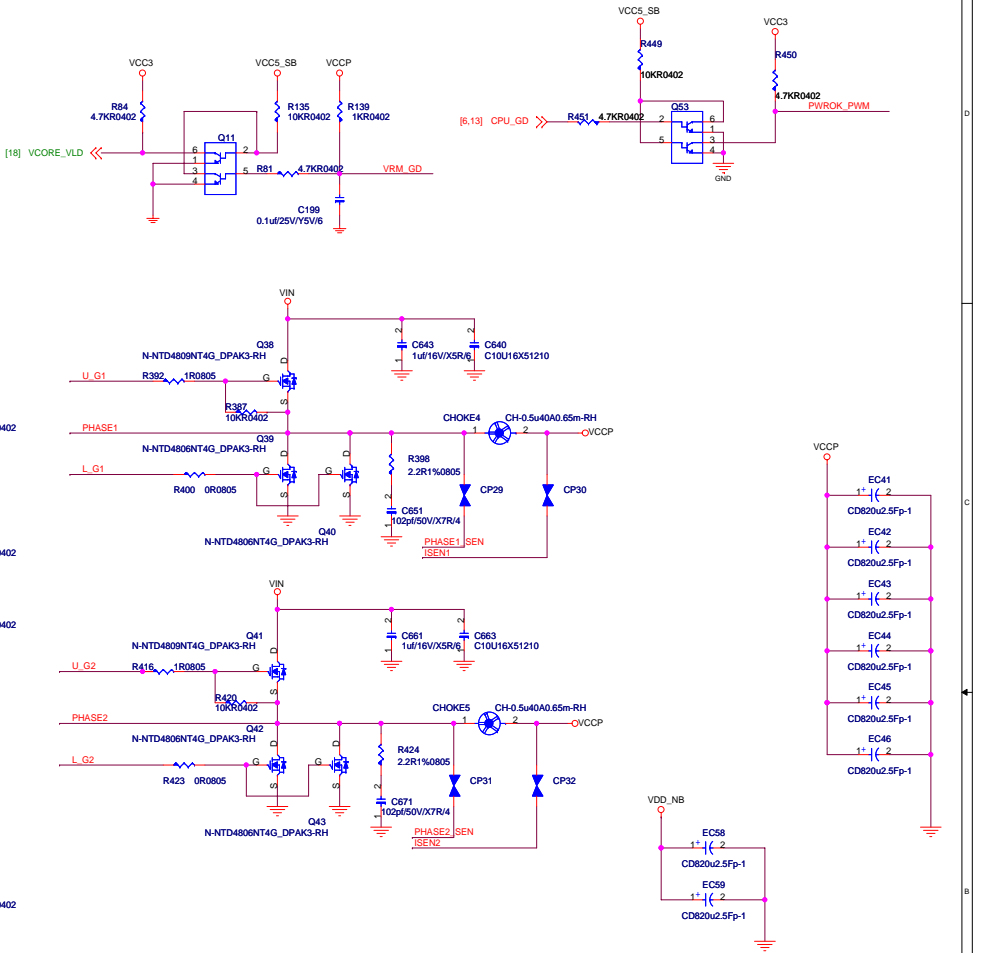
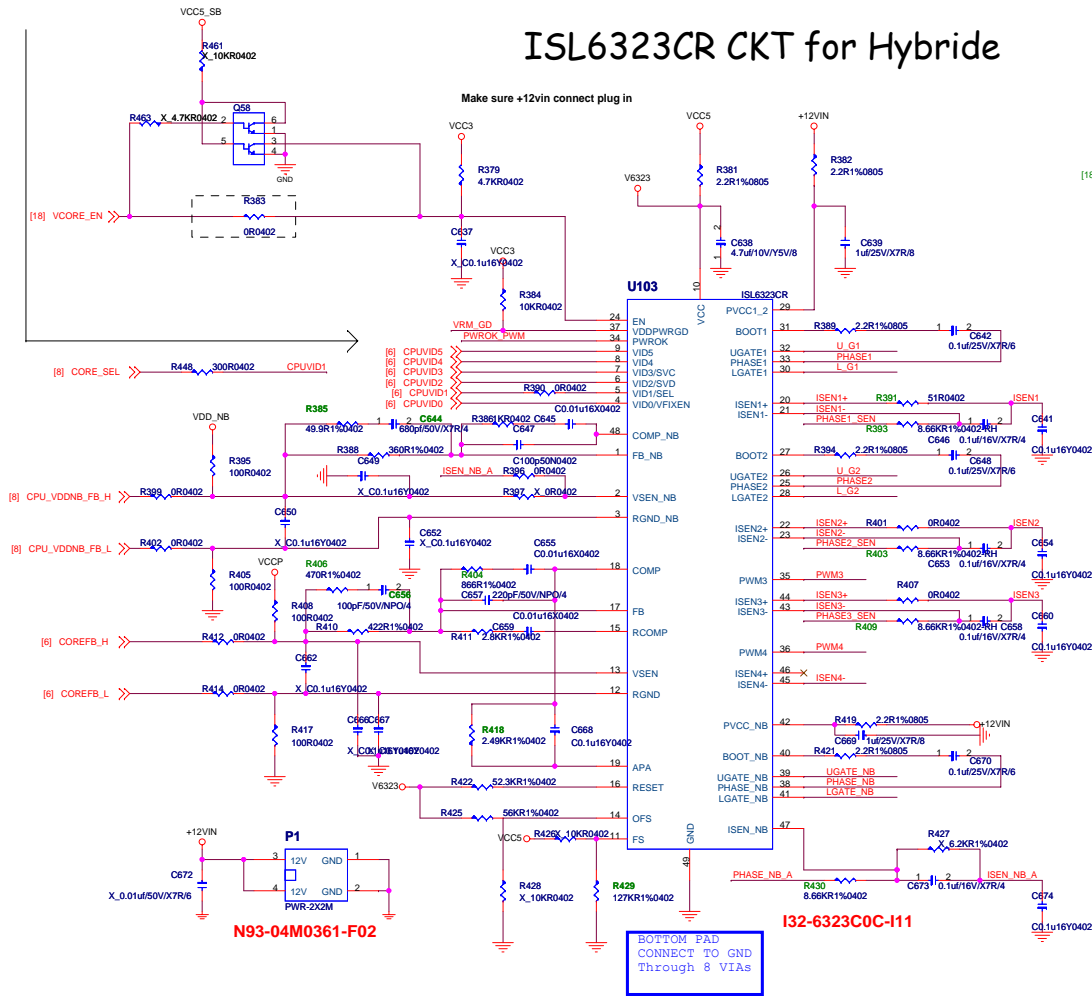
C166 C68p50N0402-RH

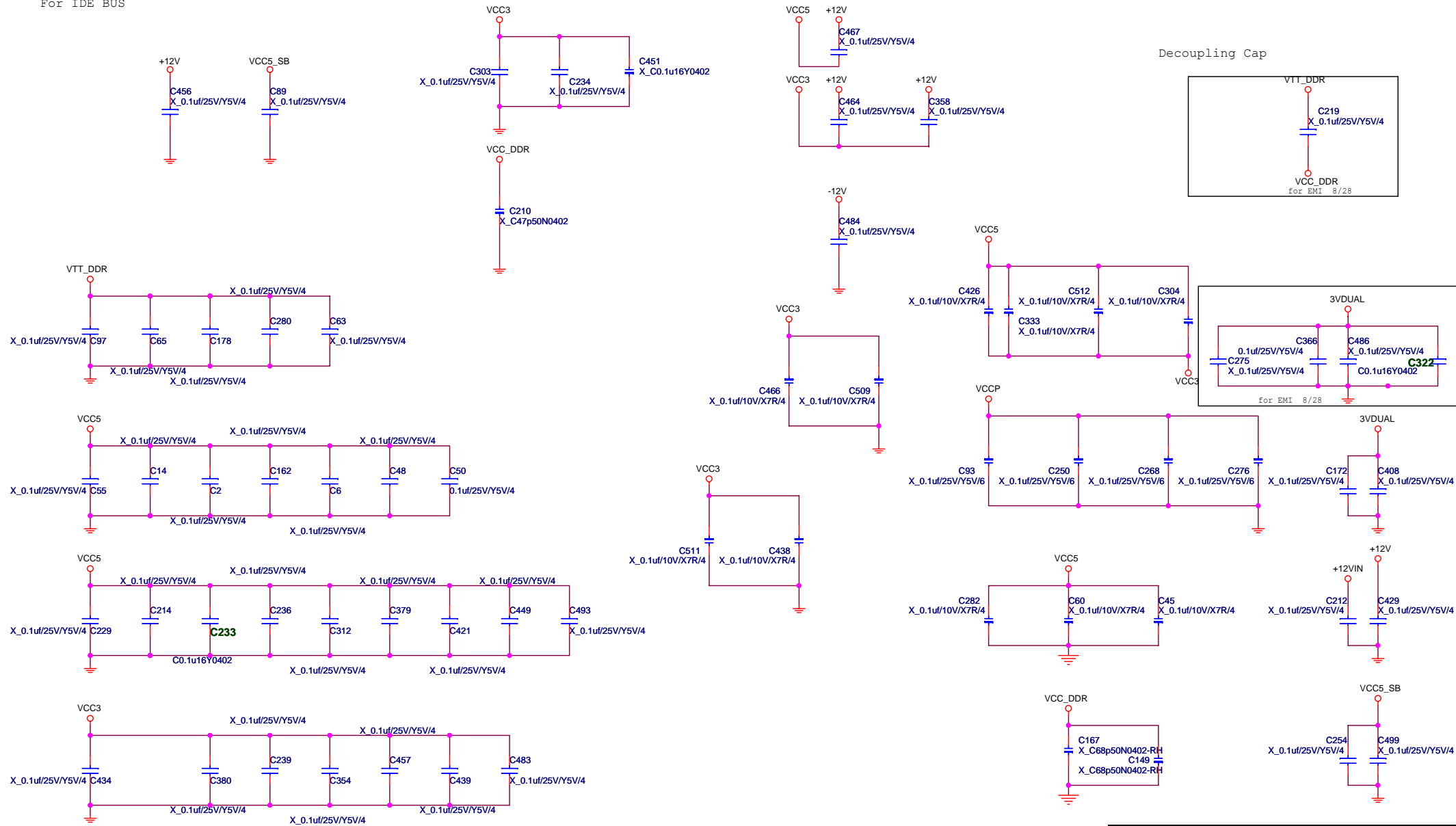
C147 X_C68p50N0402-RH

change for EMI 2/18 request

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---------------------------|-----------------|-----|-----|-----|-------|
| PWROK Input LOW Threshold | | - | - | 0.8 | V |

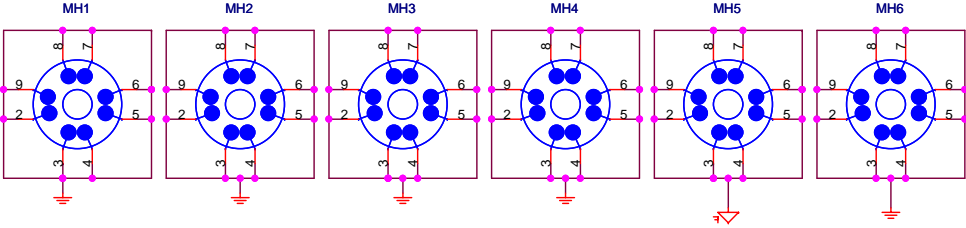
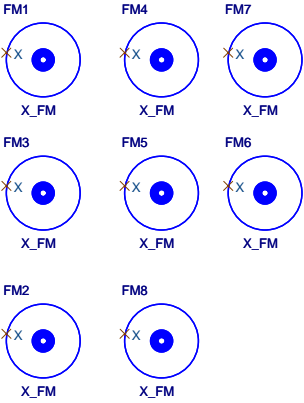
ISL6323CR KTK for Hybride





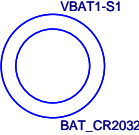
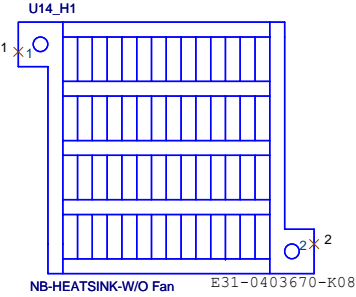
Optics Orientation Holes

Mounting Holes

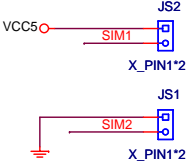


NB FAN/HEAT-SINK

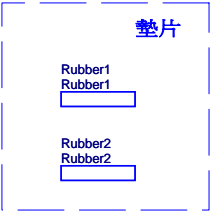
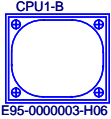
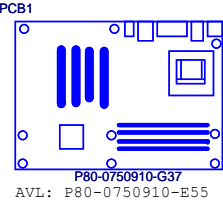
BATTERY



Simulation



PCB



Power Deliver Chart

| AM2-CPU | | |
|------------|--------------------|---------|
| 0.8V-1.55V | VDD | - 110A |
| 0.9V | VTT | - 1.75A |
| 2.5V | VDDA (VCCP.VDDA25) | - 250mA |
| 1.8V | VDDIO (VCCDDR) | - 3.6A |
| 1.2V | VLDT (VCC1_2HT) | - 1.4A |

| MCP78V | | |
|--------------------|---------------------------------|---------------------|
| 1.1V | Core Power | - 14.2A |
| 1.1V_PEA | PCI Express Analog Logic Power | - 1580mA |
| 1.1V_PED | PCI Express Digital Logic Power | - 449mA |
| 1.1V_HT_A | HyperTransport Analog Power | - 2522mA |
| 1.1V_HT_D | HyperTransport Power | - 304mA |
| 1.1V_SPA | SATA Analog Logic Power | - 365mA |
| 1.1V_SPD | SATA Digital Logic Power | - 109mA |
| 1.1V_PLL_DPPLL | HDMI PLL Power | - 12mA |
| 1.1V_PLL_PE_SS | PCI Express SS PLL Power | - 17mA |
| 1.1V_PLL_PE | PCI Express PLL Power | - 197mA |
| 1.1V_PLL_SP_VDD | SATA PLL Power | - 159mA |
| 1.1V_PLL_SP_SS | SATA Spread-Spectrum PLL Power | - 12mA |
| 1.1V_PLL_HT | Hyper Transport PLL Power | - 150mA |
| 1.1V_PLL_CPU | HT PLL Power | - 17mA |
| 1.1V_PLL_DISP | iGPU Display PLL Power | - 40mA |
| 1.1V_PLL_LEG | Legacy Logic PLL Power | - 20mA |
| 1.1V_PLL_MAC_DUAL | MAC PLL Power | - 6mA |
| 1.1V_DUAL | Core Auxiliary Power | - 280mA |
| 3.3V | I/O Power | - 720mA |
| 3.3V_HDMI | HDMI I/O Power | - 300mA |
| 3.3V_RGB_DAC | RGB DAC Power | - 104mA |
| 3.3V_PLL_USB | USB PLL Power | - 19mA |
| 3.3V_DLL_HT | Hyper Transport DLL Power | - 74mA |
| 3.3V_HDMI_PLL_HVDD | HDMI PLL Power | - 8mA |
| 3.3V_VBAT | RTC Power | - 10mA@G3 5mA@S0 |
| 3.3V_DUAL | I/O AUX Power | - 32mA |
| 3.3V_USB_DUAL | USB AUX logic | - 523mA |

| Audio ALC888 | | |
|--------------|------|--------|
| 3.3V | DVDD | - 0.3A |
| 5V | AVDD | - 0.1A |

| LAN RTL8211BL | | |
|---------------|--------------|---------|
| 3.3V | VDD33/AVDD33 | - 65mA |
| 1.8V | AVDD18 | - 103mA |
| 1.5V | DVDD15 | - 241mA |

| ISL6323CR -U103 | | |
|-----------------------|------------|--|
| VCCP | 0.8V-1.55V | |
| 3-Phase+1 Switch 110A | | |

| UP7711 -U11 | | |
|-------------|------|--------------|
| VTT_DDR | 0.9V | Linear 2.35A |

| L1087 -U4 | | |
|-----------|------|--------------|
| VDDA_25 | 1.2V | Linear 250mA |

| UP6103 SW -U10 | | |
|----------------|------|-------------|
| VCC_DDR | 1.8V | PWM 33.509A |

| LM358 | | |
|-----------------|------|----------------|
| VCC1.5 -U19B | 1.5V | Linear 21.559A |
| VCC1_2HT -U107A | 1.2V | Linear 1.4A |
| VCC1.2 -U19.A | 1.1V | Linear 20.159A |

| UP7707 -U24 | | |
|-------------|------|--------------|
| 1.2VDUAL | 1.1V | Linear 280mA |

| UP7501 -U7 | | |
|------------|----|---------------|
| 5VDIMM | 5V | Switch 9.049A |

| UP7533 -U13 | | |
|------------------|----|---------------|
| 5VUSB_REAR/FRONT | 5V | Linear 6.345A |

| UP7706 -U105 | | |
|--------------|------|---------------|
| 3VDUAL | 3.3V | Linear 2.744A |

| DDRIII x4 & TERMINATOR | | |
|------------------------|-----------------|--------|
| 0.9V | VTT_DDR | - 0.6A |
| 1.8V | VCC_DDR (S0,S1) | - 6A |

| PCI Express x16 slot | | |
|----------------------|-----------|---------|
| +12V | | - 5.5 A |
| +3.3Vaux | (wake) | - 375mA |
| +3.3Vaux | (no wake) | - 20mA |
| +3.3V | | - 3.0A |

| PCI Express x 1 slot | | |
|----------------------|-----------|---------|
| +12V | | - 0.5 A |
| +3.3Vaux | (wake) | - 375mA |
| +3.3Vaux | (no wake) | - 20mA |
| +3.3V | | - 3.0A |

| PCI slot x2 | | |
|-------------|-----------|---------|
| +3.3Vaux | (wake) | - 750mA |
| +3.3Vaux | (no wake) | - 40mA |
| +3.3V | | - 15.2A |
| +5V | | - 10A |
| +12V | | - 1A |

| USB x12 | | |
|---------|---------|--------|
| +5V | (S0,S1) | - 6.0A |
| +5V | (S3) | - 20mA |


| PS2 | | |
|-----|---------|---------|
| +5V | (S0,S1) | - 345mA |
| +5V | (S3) | - 2.0mA |

| | | |
|---------|------|-------|
| 5VAudio | +5VR | 200mA |
|---------|------|-------|

| | |
|---------|--|
| +12V | |
| ATX 2x2 | |

| | | | | | | | |
|-----------|--------|-------|---------|-------|------|------|--|
| +5V | 28.38A | +3.3V | 25.469A | +5VSB | 7.2A | +12V | |
| ATX POWER | | | | | | | |

■ Bead or Inductor
 ▤ X-Copper


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Link to the Future

Title: POWER DELIVERY

| | | |
|--------|--------------------|-----|
| Size | Document Number | Rev |
| Custom | MS-7509 2008/09/01 | 20 |

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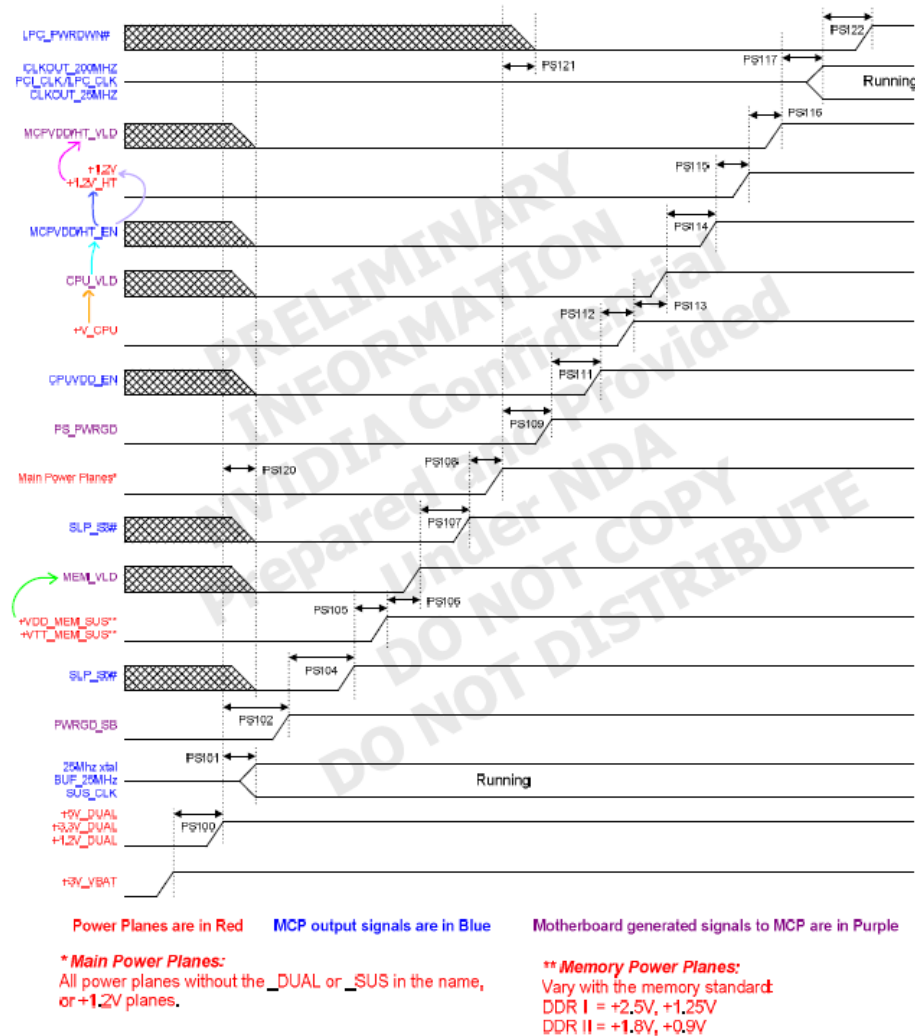


Figure 4-2. MCP68 G3-to-S0 Power-Up Sequence

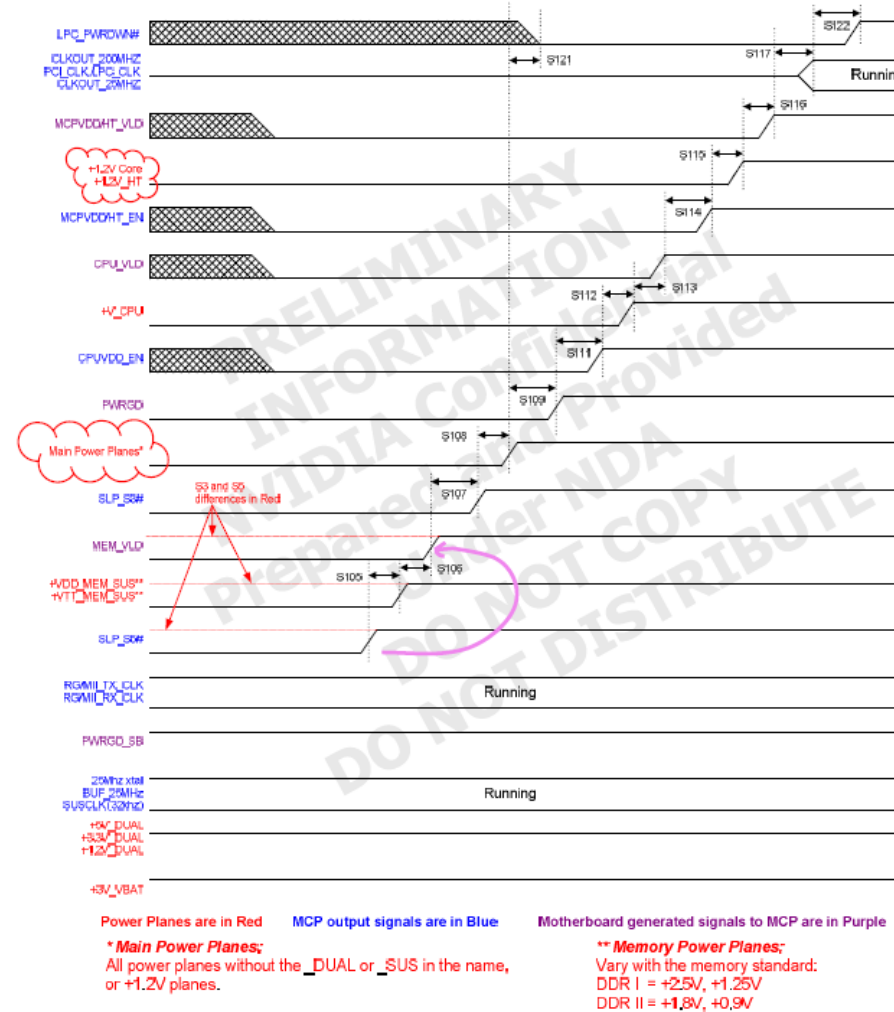


Figure 4-3. MCP68 S3/S4/S5 Power Resume Sequence

2008/1/10 0A CHANGE 10

| 項目 | 原 因 | 元 件 |
|----|------------------------------------|---|
| 1 | AMD CPU request | Add R354 and R191 |
| 2 | for NVIDIA circuit D version | U14 V22 pin circuit modify |
| 3 | for no JMP381 install | Add R196 |
| 4 | for UPI7501 挑 700W power | Q33 and Q34 and R350 and R351 and R352 |
| 5 | for chipset ver:A2 circuit modify | Q27, Q28, R228, R233, R329, R234, R349 and add R16,R320 |
| 6 | signal quality | R244 and R245 |
| 7 | HT_VLD and VCC1.2 timing | R319 and C422 |
| 8 | G3 to G5 VCC_DDR have power output | Add Q36, D32, R322, R323 |

2008/8/11 10 CHANGE 20

- 1.Add Front USB*2 ,Rear USB*2
- 2.Change Page32. VRM-ISL6566 to VRM-ISL6323CR
- 3.Change E-SATA+USB to N58-15M0021-L06
- 4.Change Parallal Port to Pin Head
- 5.Serial Port to Pin Head
- 6.Change U11 to UPY□11U8

2008/8/12

- 1.Change
L04-25B7021-L65*3: output choke of vcore
L04-05A7211-L65*1: output choke of NB
L04-12A7321-L65*1: input choke of vcore
C94-10216A1-TA0*4:input CAP of vcore
C94-1820641-TA0*8: output CAP of vcore
- 2.Add U107A VCC1.5->VCC1_2HT

2008/8/13

- 1.Change
Q35 to D03-0903BDB-N03

2008/8/14

- 1.Change
R281 to 0603
1394&USB to N58-14M0031-L06
Update VCC_DDR input Cap footprint

2008/8/15

- 1.Change
R123.R124 to 1K
R27.R29 to 15R1%
- 2.SWAP
RN53
RN53.1 N78884922
RN53.2 LINE2_L_JAUD
RN53.3 N78885015
RN53.4 LINE2_R_JAUD
RN53.5 N78884943
RN53.6 MIC2_R_JAUD
RN53.7 N78884953
RN53.8 MIC2_L_JAUD
CN3
CN3.2RACK#
CN3.4RBUSY
CN3.6RPE
CN3.8RSLCT
- RN3
RN3.1RACK#
RN3.3RBUSY
RN3.5RPE
RN3.7RSLCT
CN4
CN4.2PRND4
CN4.4PRND5
CN4.6PRND6
CN4.8PRND7
RN6
RN6.1PRD7
RN6.2PRND7
RN6.3PRD6
RN6.4PRND6
RN6.5PRD5
RN6.6PRND5
RN6.7PRD4
RN6.8PRND4
- RN5
RN5.1PRND4
RN5.3PRND5
RN5.5PRND6
RN5.7PRND7
CN5
CN5.2PRND0
CN5.4PRND1
CN5.6PRND2
CN5.8PRND3
RN10
RN10.1PRD3
RN10.2PRND3
RN10.3PRD2
RN10.4PRND2
RN10.5PRD1
RN10.6PRND1
RN10.7PRD0
RN10.8PRND0
- RN8
RN8.1PRND0
RN8.3PRND1
RN8.5PRND2
RN8.7PRND3
CN6
CN6.2STB#
CN6.4AFD#
CN6.6PINIT#
CN6.8SLIN#
RN12
RN12.1RSLIN#
RN12.2SLIN#
RN12.3RINIT#
RN12.4PINIT#
RN12.5RAFD#
RN12.7RSTB#
RN12.8STB#
RN11
RN11.1STB#
RN11.3AFD#
RN11.5PINIT#
RN11.7SLIN#

2008/8/20

- 1.ADD D31
- 2.De1 D5.FS1

2008/8/22

- 1.SWAP
U14
RN34.7 USBN2
RN34.5 USBP2
RN34.3 USBN3
RN34.1 USBP3
RN32.7 USBN0
RN32.5 USBP0
RN32.3 USBN1
RN32.1 USBP1
RN52
RN52.5 WP#
RN52.3 TRACK0#

2008/8/16

- 1.SWAP
RN33
RN33.1 USBP10
RN33.2 SBD10+
RN33.3 USBN10
RN33.4 SBD10-
RN33.5USBP11
RN33.6 SBD11+
RN33.7 USBN11
RN33.8 SBD11-
RN59
RN59.1 USBP1
RN59.2 SBD1+
RN59.3 USBN1
RN59.4 SBD1-
RN59.5USBP0
RN59.6 SBD0+
RN59.7 USBN0
RN59.8 SBD0-
D37.1 SBD1-
D37.3 SBD0-
D37.6 SBD1+
D37.4 SBD0+
D19.1 SBD11-
D19.3 SBD10-
D19.6 SBD11+
D19.4 SBD10+
LAN_USBA.6 SB11-
LAN_USBA.7 SB11+
LAN_USBA.2 SB10-
LAN_USBA.3 SB10+
I1394_USB1B.6 SB2-
I1394_USB1B.7 SB2+
I1394_USB1B.2 SB3-
I1394_USB1B.3 SB3+

2008/8/25

- 1.ADD R462.R488.C88
- 2.Change R430 4.32K->8.66K
- 3.Change R393 & R403 & R409 4.32K->5.36K
- 4.Q9 -S connect VCC5_SB and D connect 5VDIMM

2008/8/26

- 1.Change ATX1 N93-24M0131-H06 to N93-24M0131-L06

2008/8/27

- 1.ADD C83

2008/8/28

- 1.ADD RN60.RN61
- 2.1.ADD L15.L16.L17.L18.L19.L20.L21.L22.L23.L24.L25.L26

2008/8/29

- 1.ADD Q37.FM8
- 2.DEL D31.C313

2008/9/1

- 1.Change R380->1K R17->35.7K R16->38.3K R234->2K

2008/9/12

- 1.ADD C424.C423.C450.U22.R266.R267.EC26
- 2.DEL R281

MS 7509-V20

2008/11/05

1394 remove

- (-)C186,C376,C420,C423,C427
- (-)C435,C450,C531,C687,C689
- (-)C692,C694 (-)C695
- (-)C424,C688,C690,C691
- (-)C381,C406 (-)C382,C431
- (-)C419,C433 (-)C436,C437
- (-)D15,D30 (-)FS2,FS3
- (-)U20 (-)U22 (-)Y4
- (-)R266 (-)R240
- (-)R246,R253(-)R267
- (-)R249(-)R254 (-)R257
- (-)EC26
- (+)I1394_USB1 change to N53-08M0191-F02
- (-)RN44,RN45(-)RN43

EMI

- (+)C233,C247,C315,C322,C328 (+)C330,C334,C335
- (-)C103,C120
- (+)R104,R95 change toL02-6008023-J07
- (+)R358,R363,R367,R372 change to R11-2490T12-W08

VRM


- (+)R391 change to R11-0510T12-W08
- (+)C656 change to C11-1011032-Y01
- (+)C657 change to C11-2211042-S02
- (+)Q39,Q40,Q42,Q43 change to D03-0480600-O05
- (+)Q45,Q46,Q48,Q49 (+)Q38,Q41,Q44,Q47 change to D03-0480900-O05
- (+)R404 change to R11-8660T12-W08
- (+)R418 change to R11-2491T12-Y01
- (+)R385 change to R11-499AT12-Y01
- (+)R393,R403,R409 change to R11-8661T12-W08
- (+)R429 change to R11-1273T22-Y01
- (+)C540,C541,C542,C543,C544
- (+)C547,C548,C553,C558,C559
- (+)C564,C565,C568,C569 change to C11-2267017-P01
- (+)CHOKE4,CHOKE5,CHOKE7 change to L04-05A7211-L65
- (+)EC41,EC42,EC43,EC44,EC45
- (+)EC46,EC58,EC59 change to C71-8210221-S03
- (+)EC50,EC51,EC52,EC53,EC54 change to C71-27116A1-N07
- (+)C644 change to C11-6812812-W08
- (+)R406 change to R11-0471T12-W08

溫度

- (+)R239 change to R11-0301T12-Y01
- (+)Q22 change to D03-0480600-O05

OTHER

- (+)EC31 change to C93-1012511-G01
- (+)R17 change to R11-0363T12-W08
- (+)Rubber1,Rubber2 E25-7530010-C81 TPM
- (-)JTPM1 AUDIO
- (+)C308 change to C11-3901012-T34
- (+)C497 change to C11-2701012-W08 RTC
- (+)Y3 change to D04-0300121-K11
- (+)C314,C316 change to C11-1201013-W08

| | | |
|---|--|------------------|
|  MICRO-START INT'L CO.,LTD. | | |
| Title HISTORY | | |
| Size Custom | Document Number MS-7509 2008/09/01 | Rev 20 |
| Date: | Wednesday, November 05, 2008 | Sheet 38 of 38 |